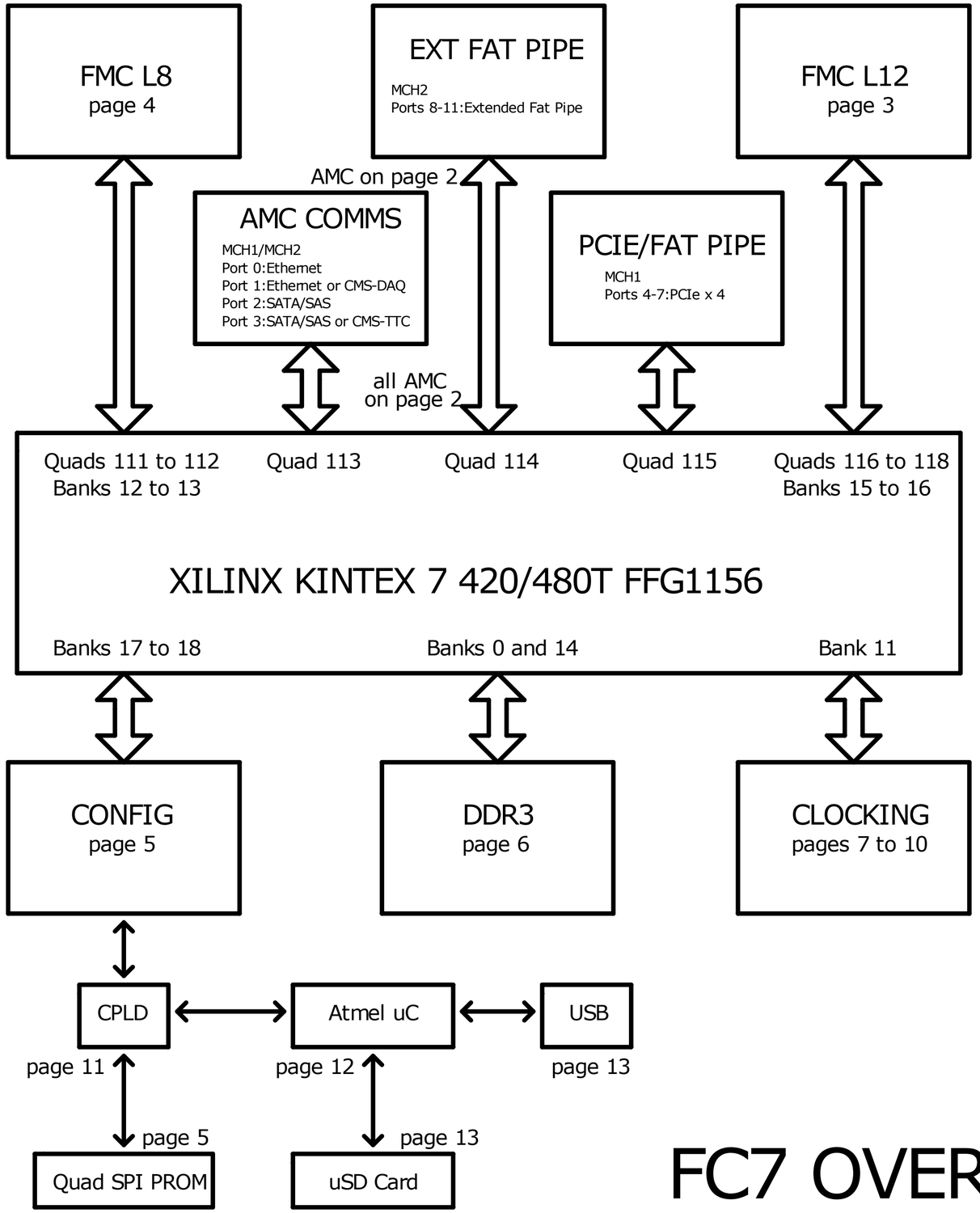
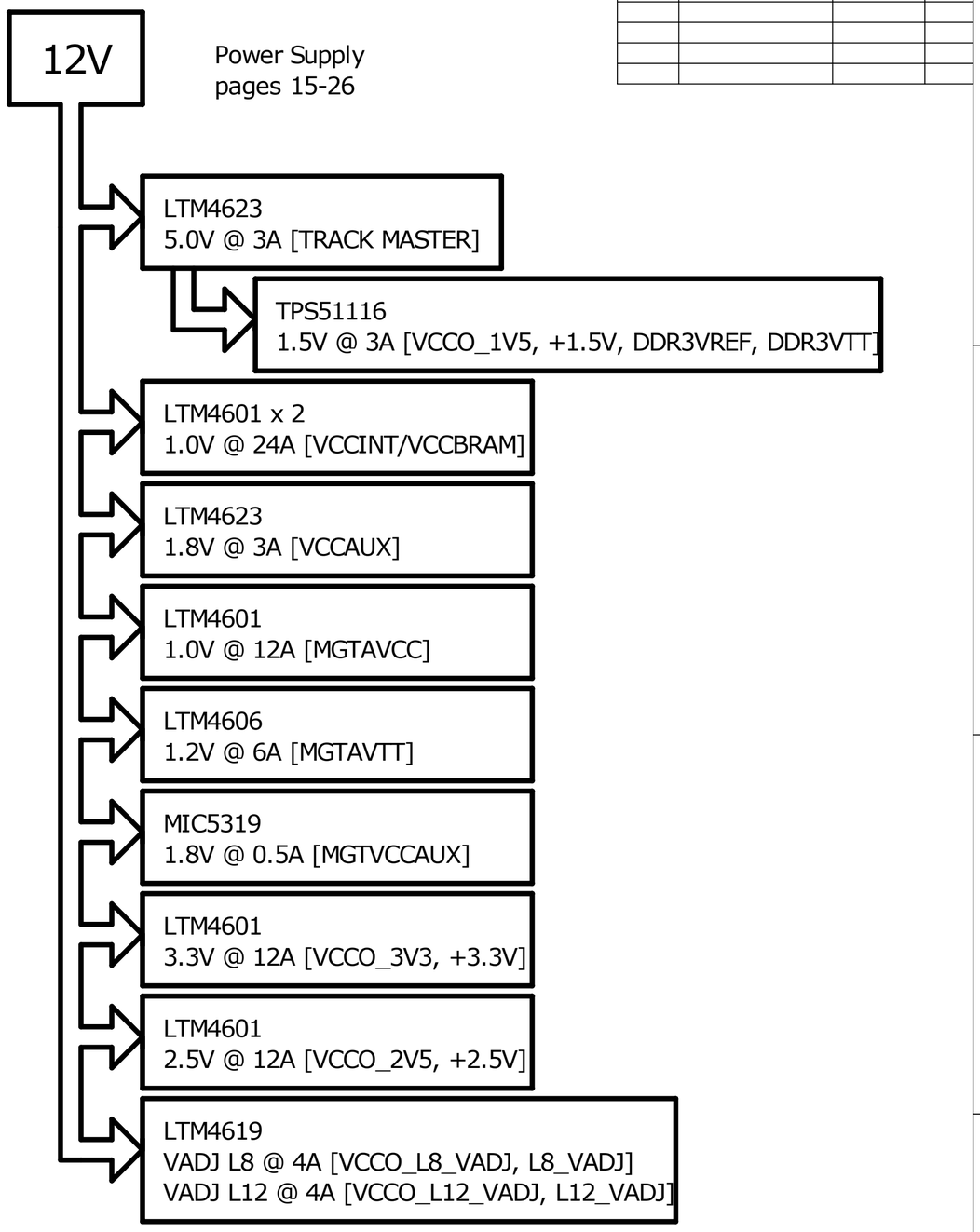
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

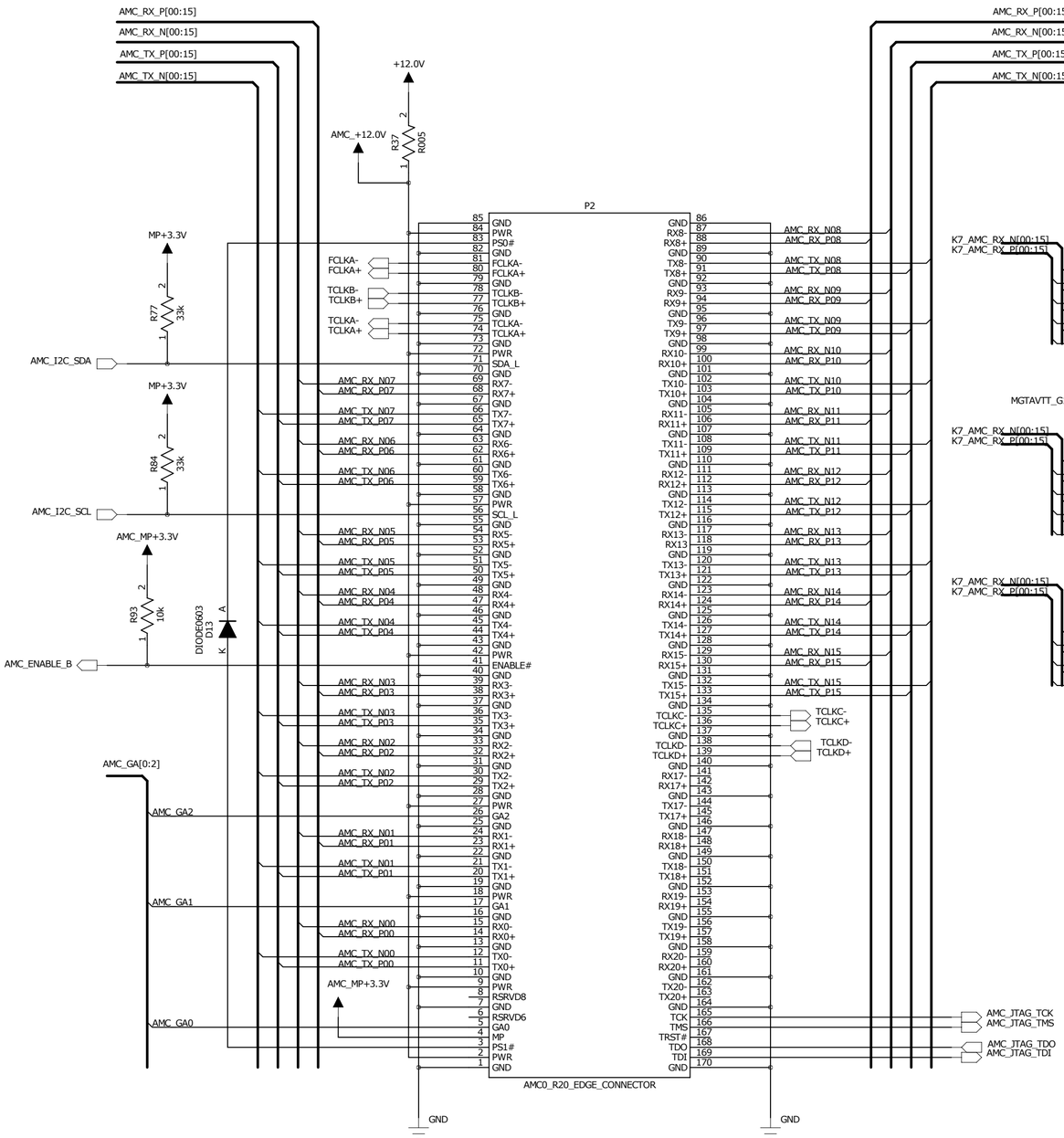


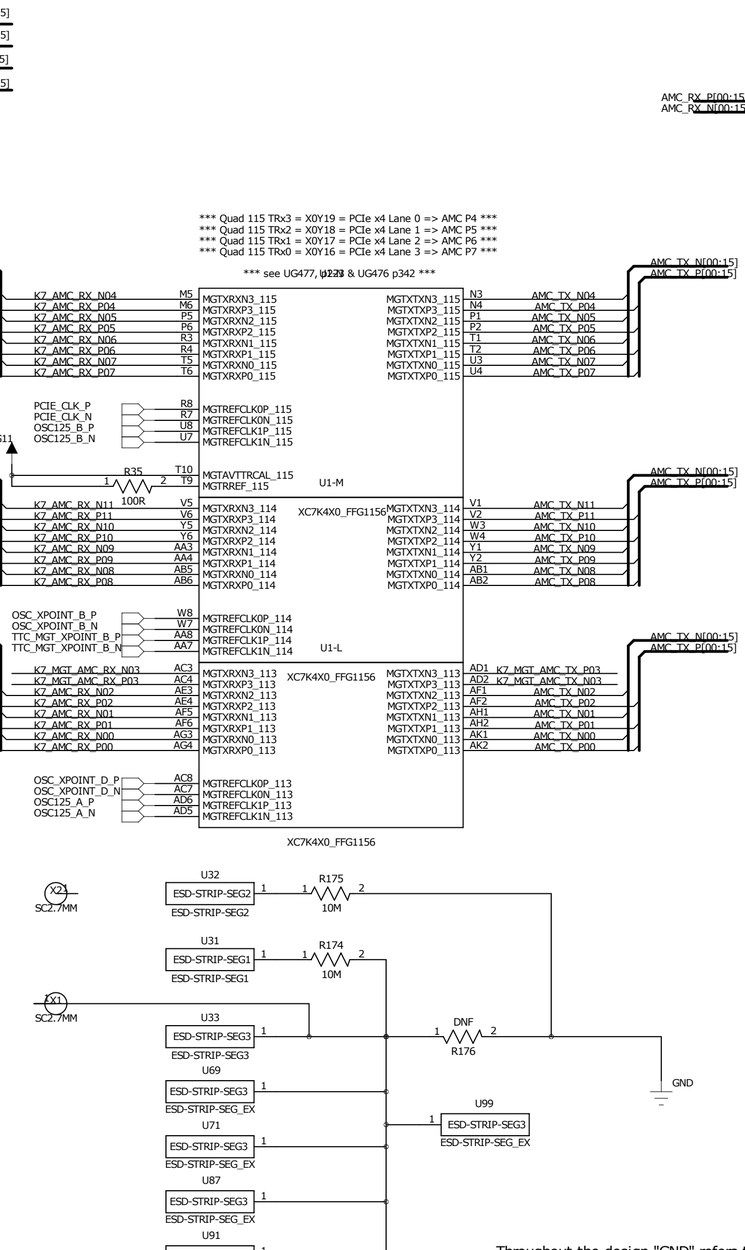


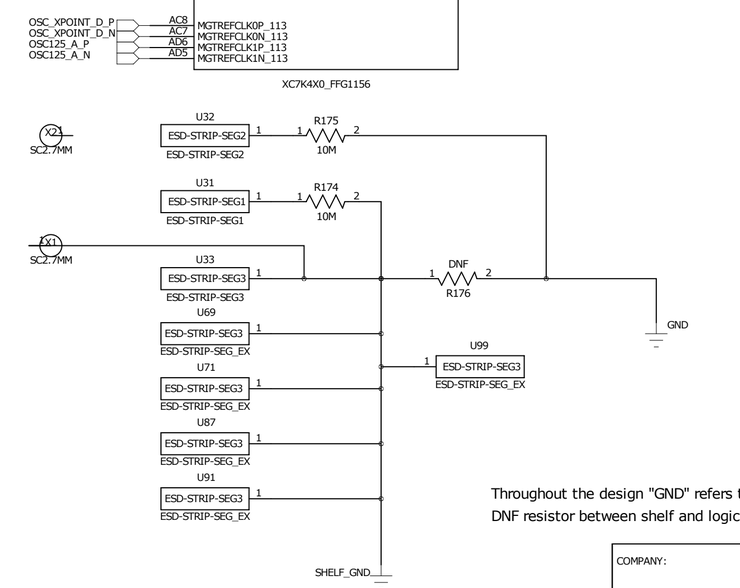
FC7 OVERVIEW

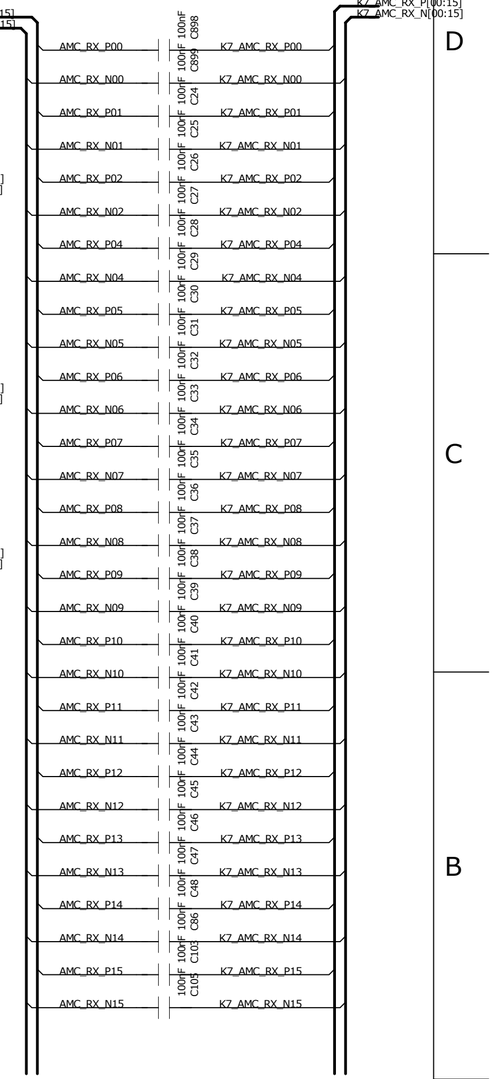
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: BOARD-OVERVIEW	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 1 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



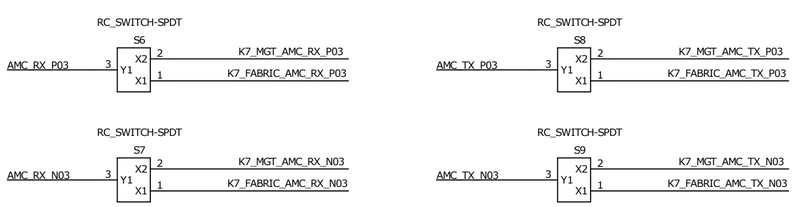






AMC Port3: FABRIC or MGT

0402 R/C switches select between FABRIC or MGT for Port 3
select FABRIC default (0R between 1 & 3)



Throughout the design "GND" refers to "Logic Ground" in the AMC spec
DNF resistor between shelf and logic ground should be located reasonably close to the face plate

24.4.13_C490/0201/100nF added. SG

DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: AMC	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 2 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

U1-F

XC7K4X0_FFG1156

U1-G

XC7K4X0_FFG1156

J106-F

FMC_CONN_HPC-LPC

J106-G

FMC_CONN_HPC-LPC

J106-H

FMC_CONN_HPC-LPC

J106-A

FMC_CONN_HPC-LPC

J106-B

FMC_CONN_HPC-LPC

J106-E

J106-D

FMC_CONN_HPC-LPC FMC_CONN_HPC-LPC

U1-Q

U1-P

U1-O

XC7K4X0_FFG1156

U14

SN65LVDS4

U20

SN65LVDS4

U5

SY58608U

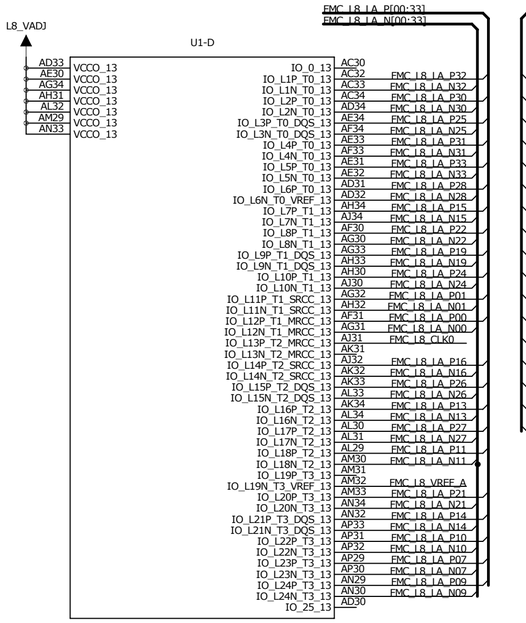
U10

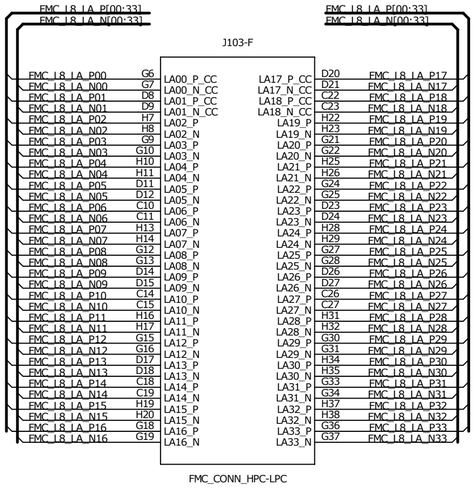
SY58608U

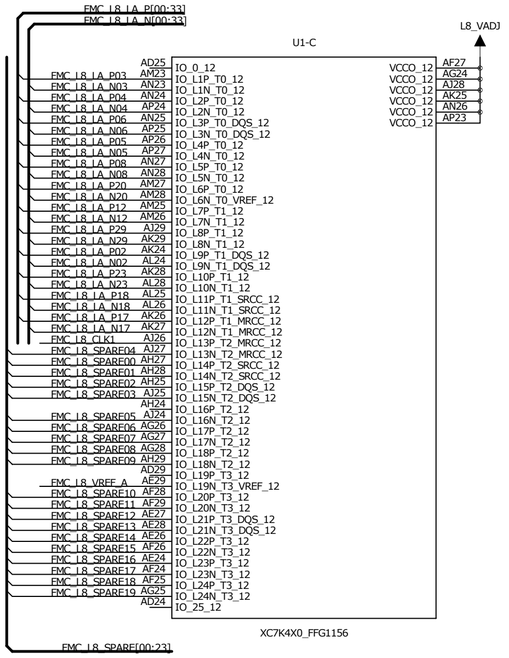
*** Place 33 ohm resistor close to FMC ***

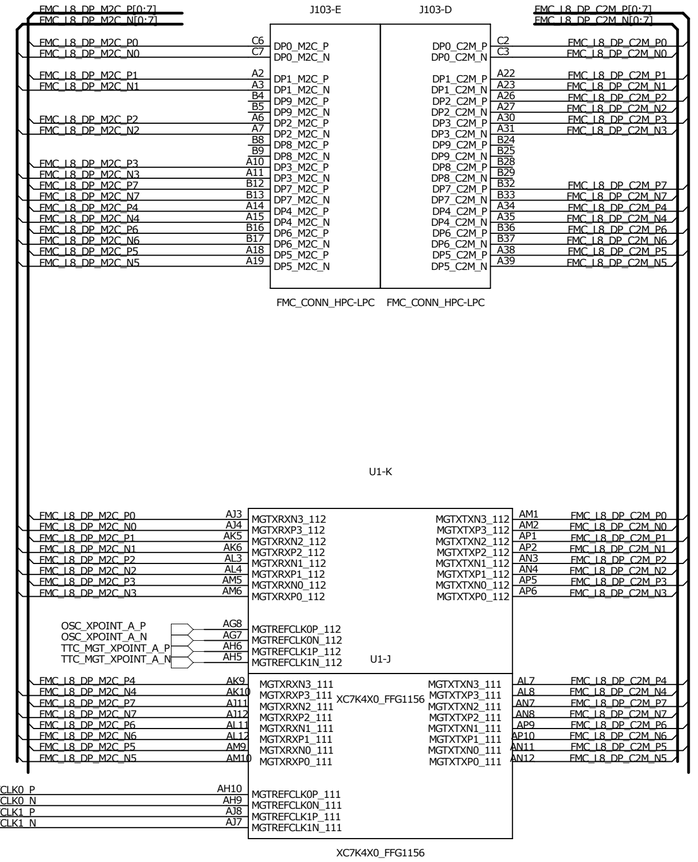
COMPANY:	Imperial College/CERN		
TITLE:	FMC_L12_IO		
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: FC7-R2	REV: v37
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 3 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





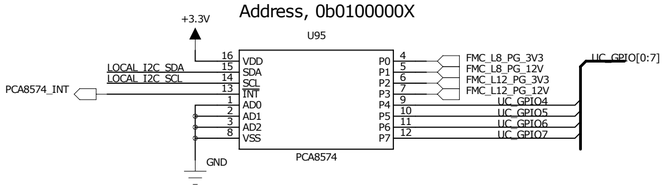


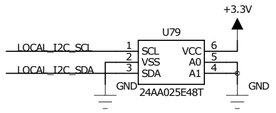


COMPANY: Imperial College/CERN			
TITLE: FMC_L8_IO			
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: FC7-R2	REV: v37
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 4 OF 26

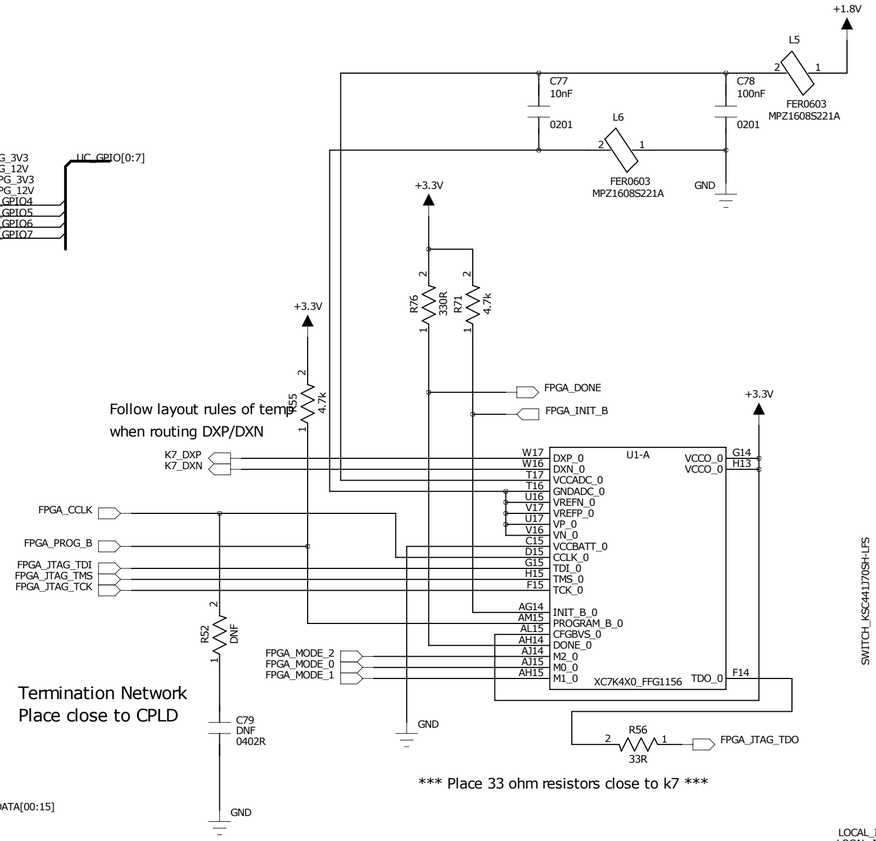
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Address, 0b0100000X

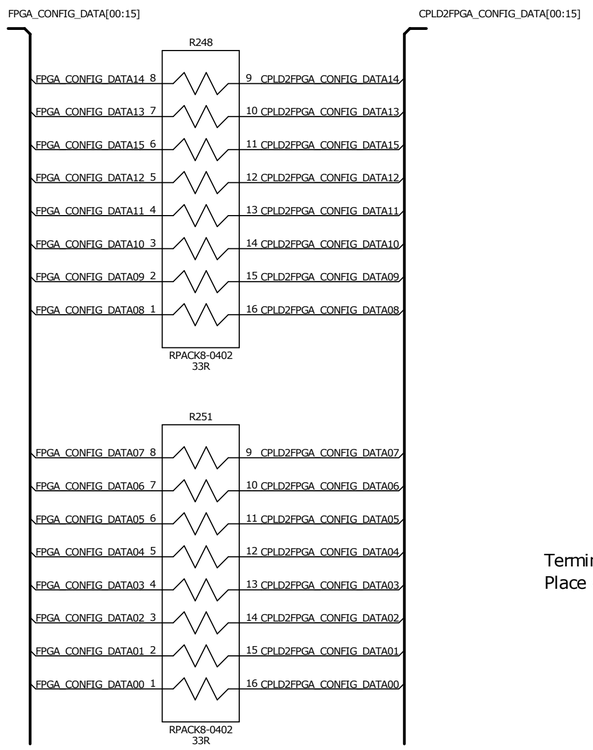


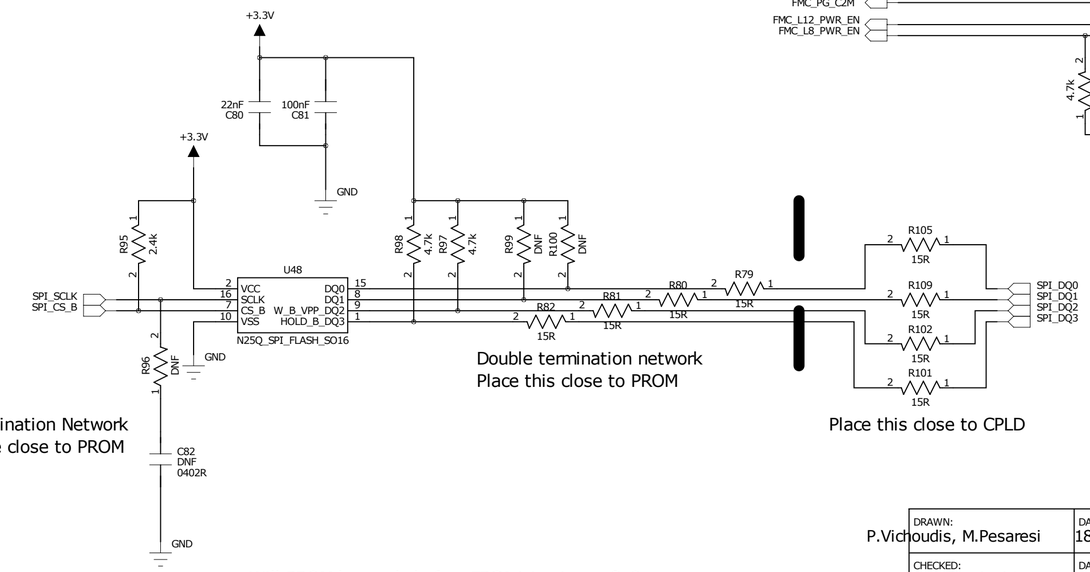


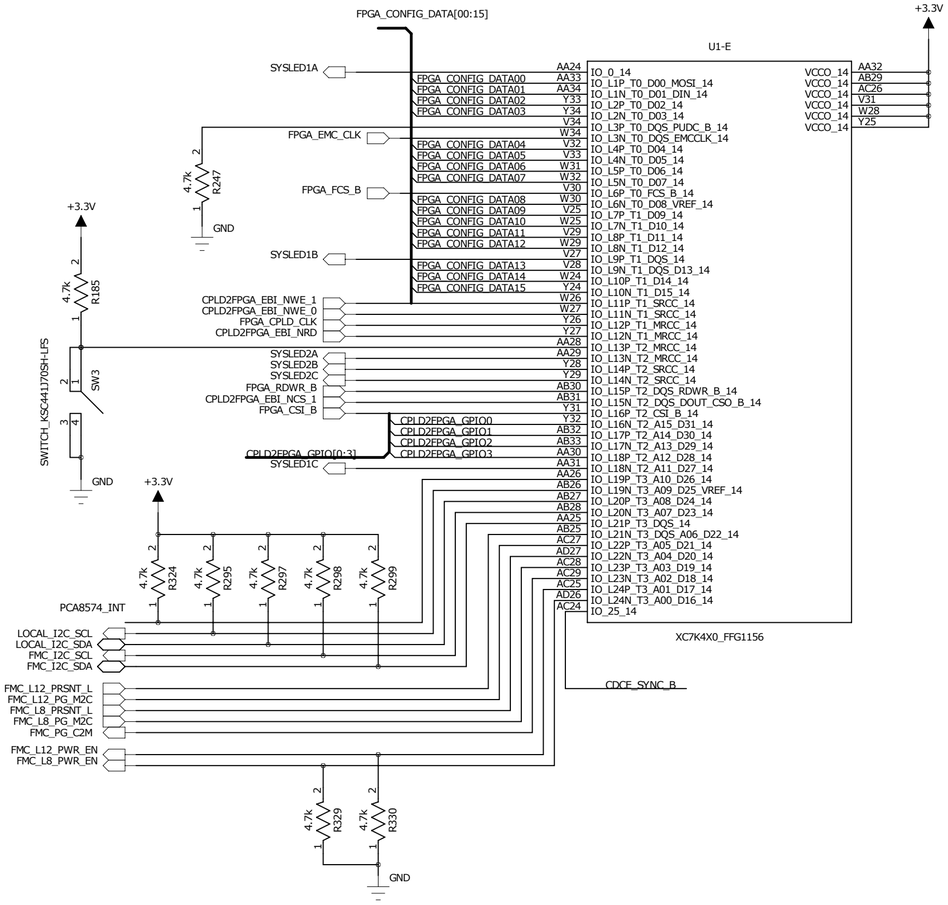
Address, 0b1010000X



RPACKs close to CPLD





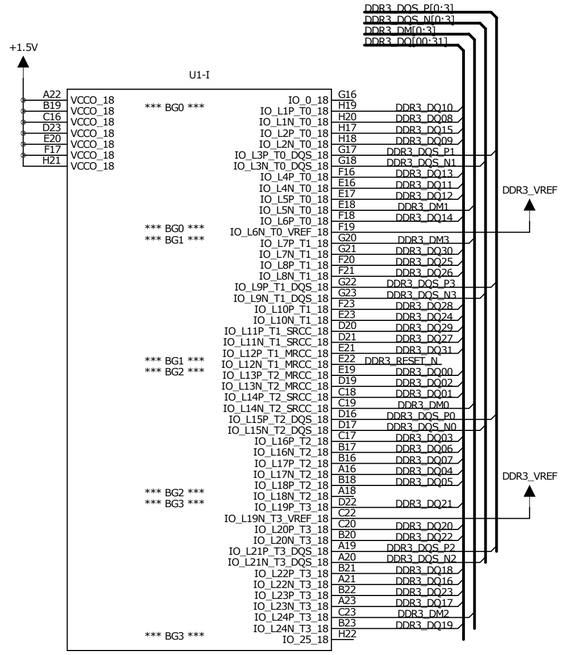


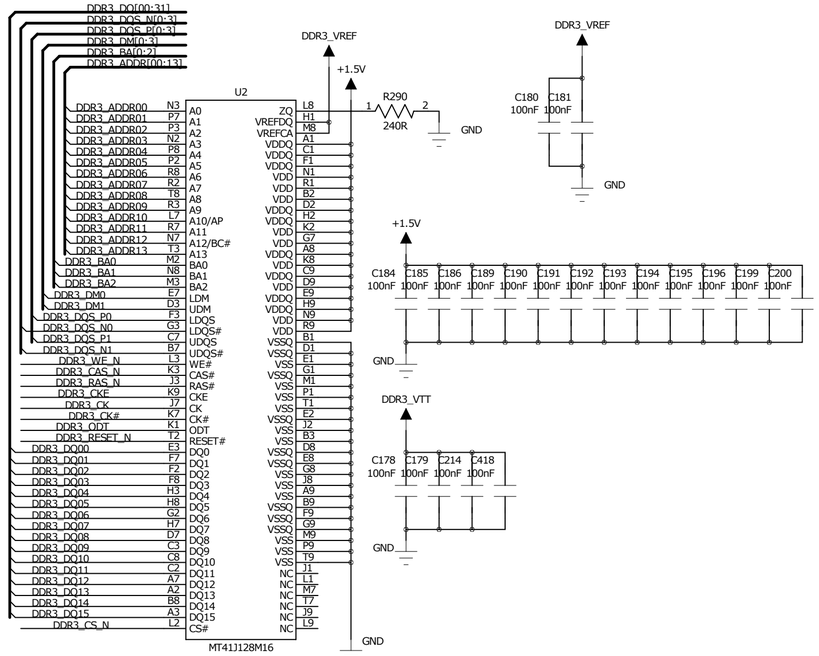
Will PROM be ready before FPGA tries to config?
CPLD can hold INIT_B or PROG_B low, but only after it has configurred.
If all else fails then CPLD restarts FPGA time X after power on...

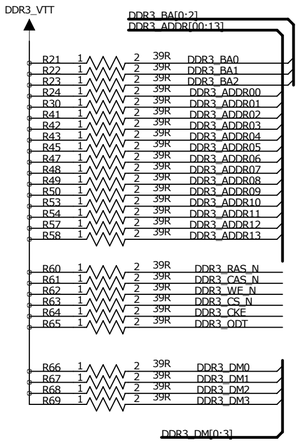
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: K7_CONFIG	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 5 OF 26

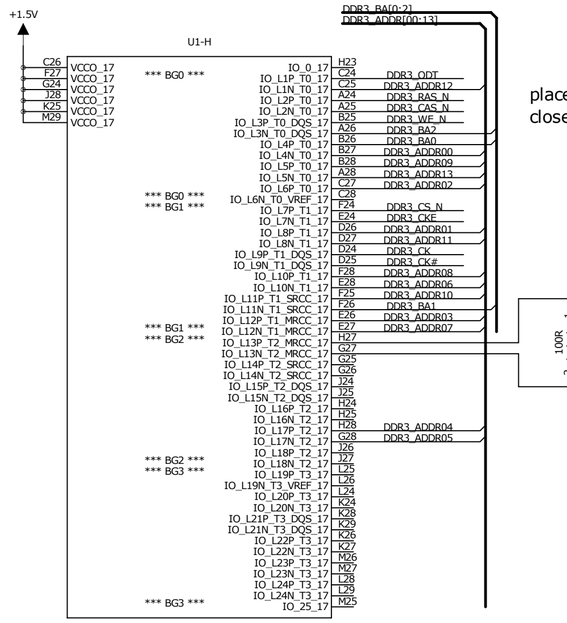
6	5	4	3	2	1

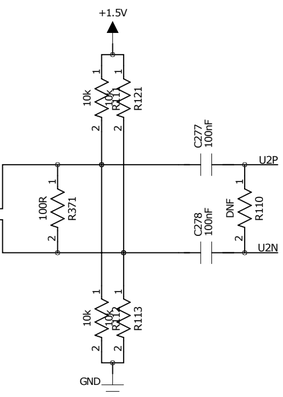
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

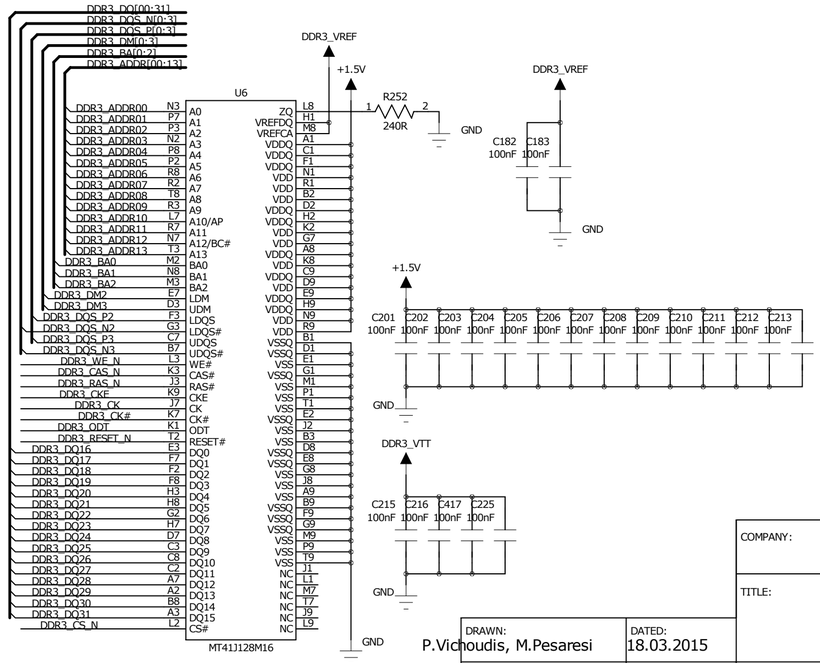






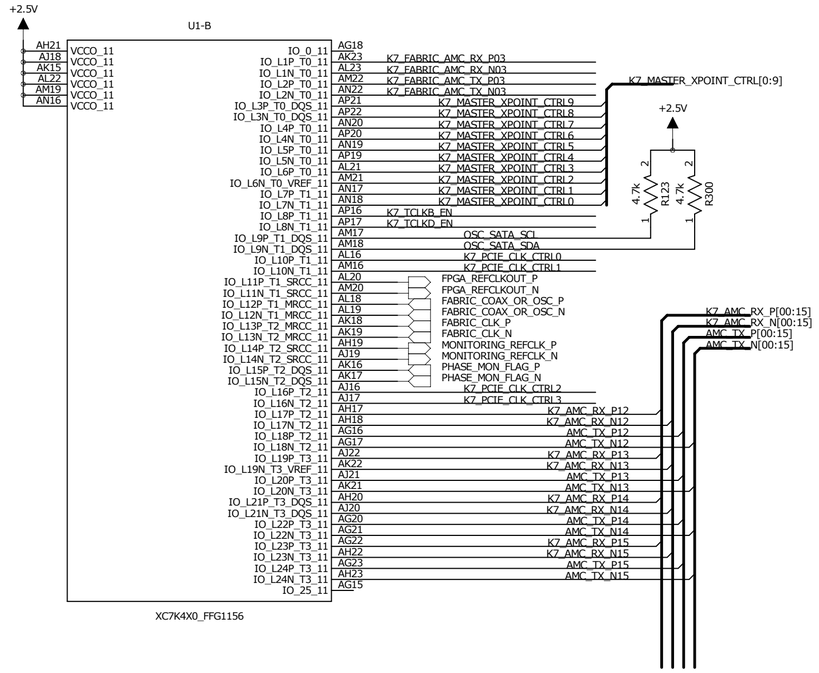


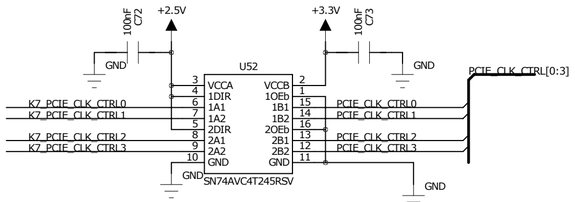


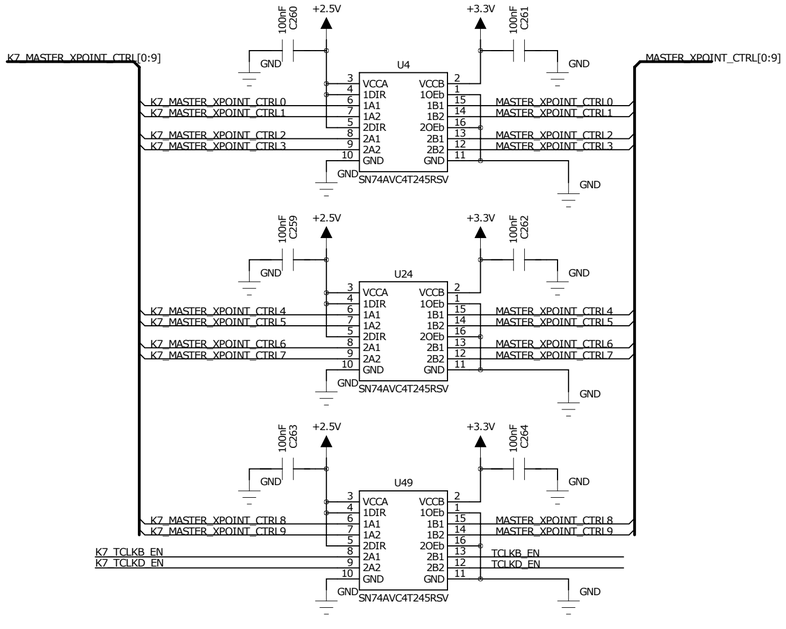


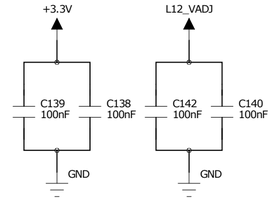
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: K7_DDR3	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
SCALE: <Scale>		SHEET: 6 OF 26	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



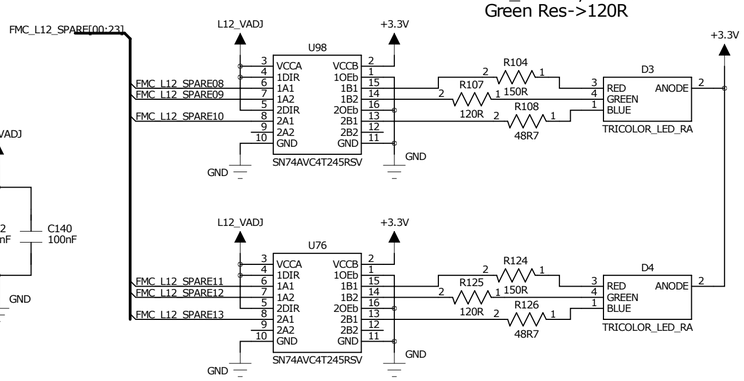


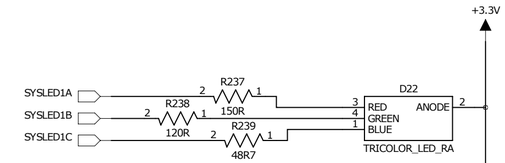


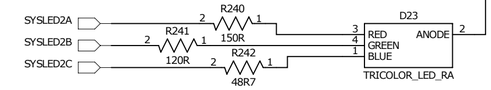


1.8V for red & green, 2.8V for blue
Aim for 10mA / LED

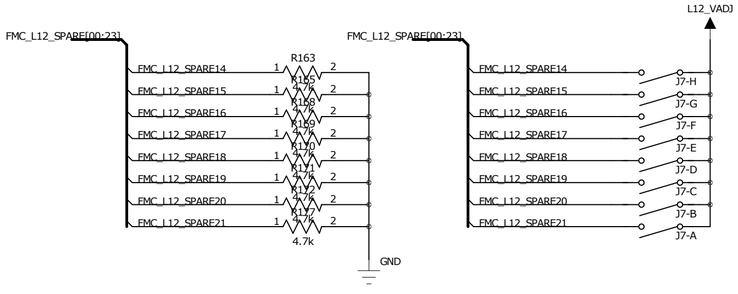
MP7_R1 Mod, AWR
Green Res->120R



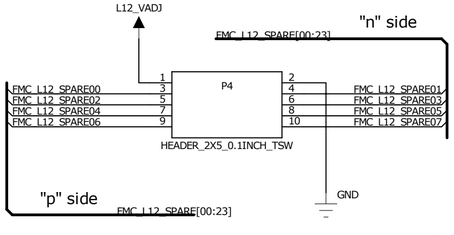


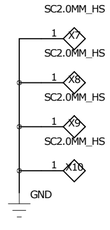


J7 gen config now pulled down externally when open



Please route as diff pairs, e.g. 0&1, 2&3, 4&5, 6&7

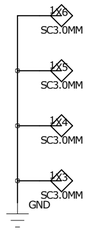




CABLE TRAY MOUNTING HOLES

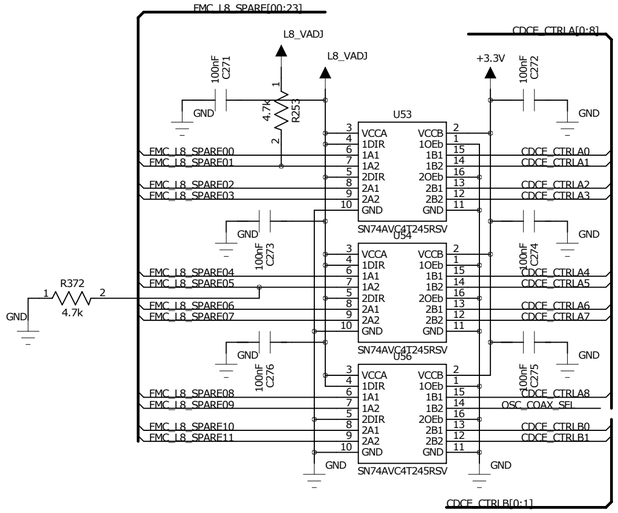
TL: X=80 , Y= 118
TR: X=131.5 , Y= 118
BL: X=80 , Y= 30.6
BR: X= 131.5 , Y= 30.6

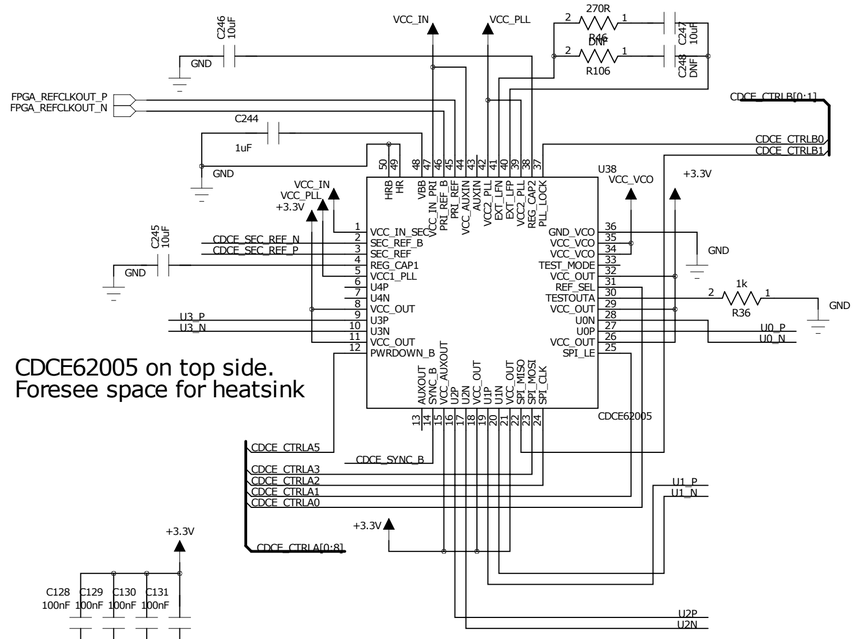
V7: X=105.2 , Y=74.3

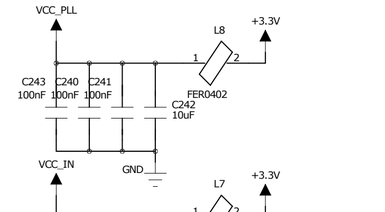


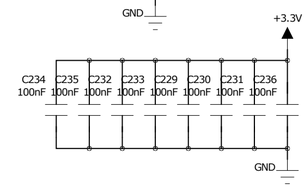
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: K7_GEN_IO	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 7 OF 26

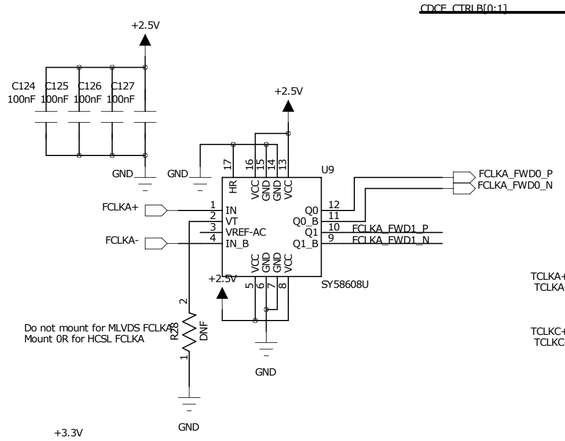
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

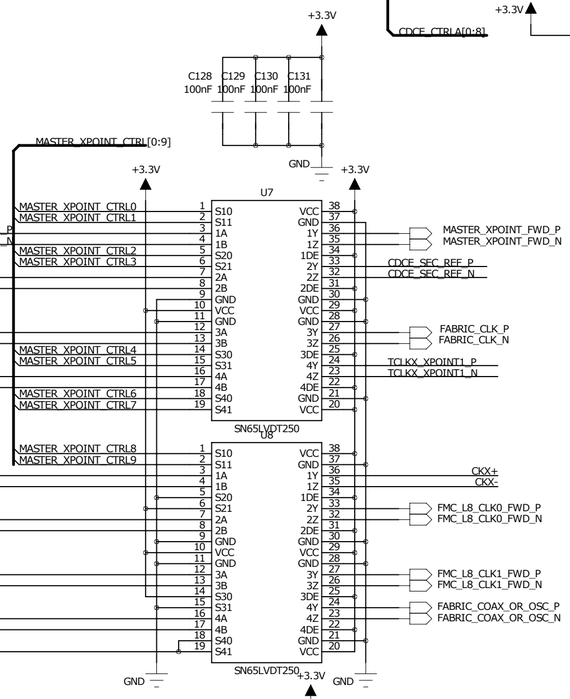


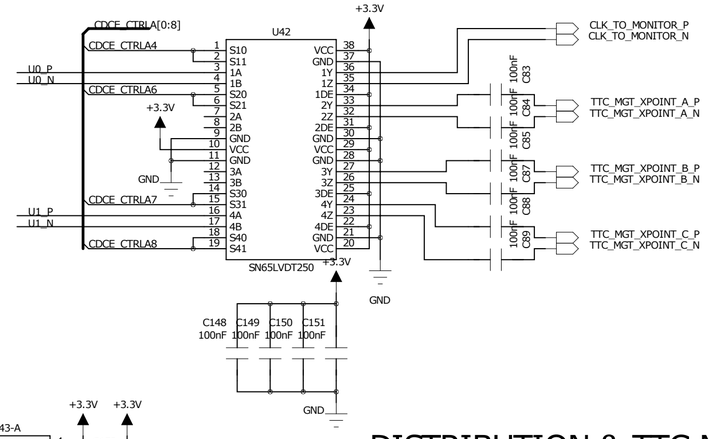


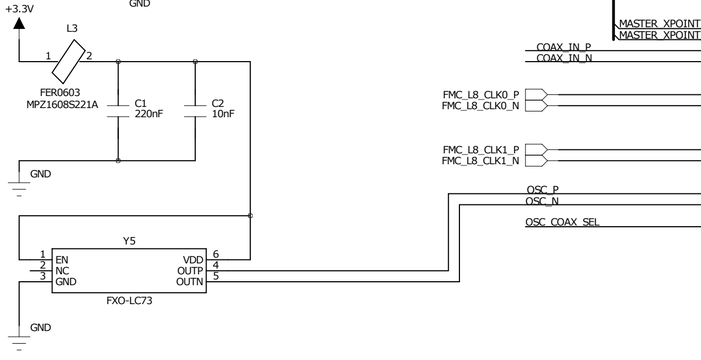


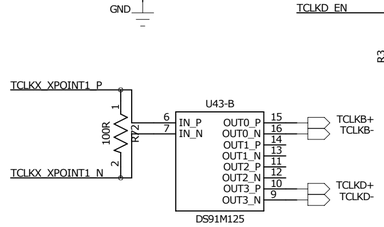


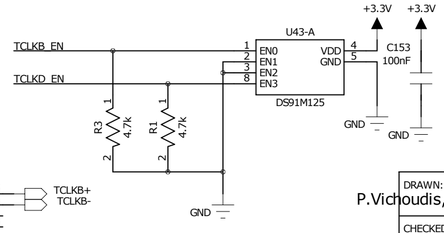


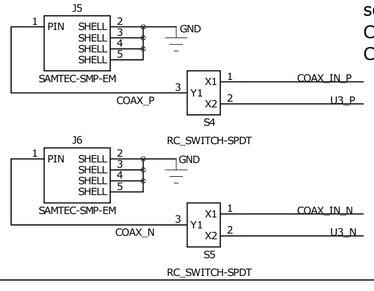










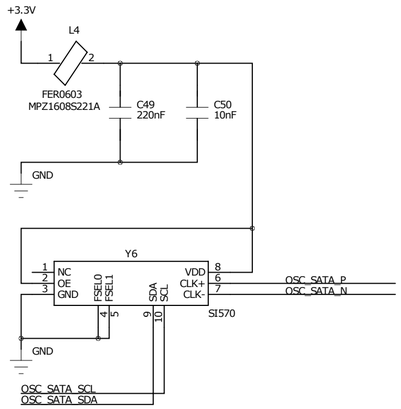


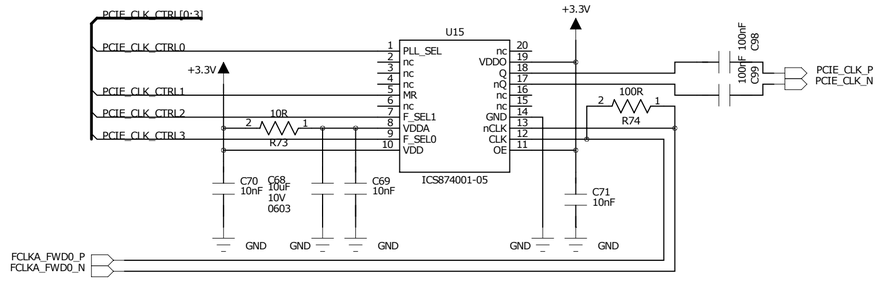
solder switches select between
COAX CLK IN or COAX CLK OUT (from CDCE)
COAX CLK IN default (0R between 1 & 3)

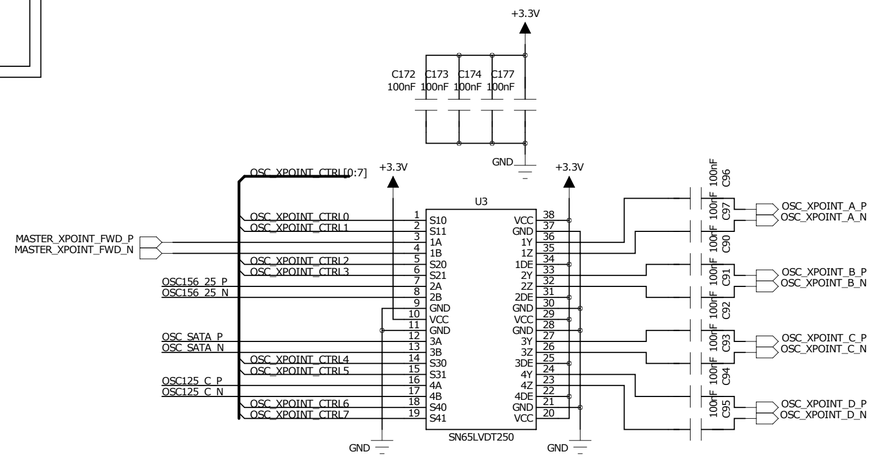
DISTRIBUTION & TTC MGT CLOCKING

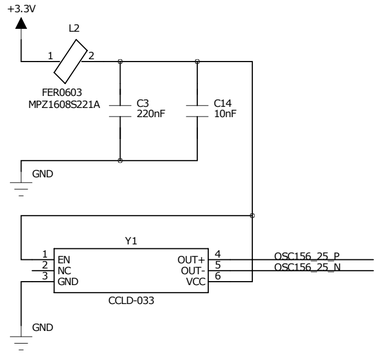
COMPANY: Imperial College/CERN			
TITLE: CLK_DIST_TTC			
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: FC7-R2	REV: v37
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 8 OF 26

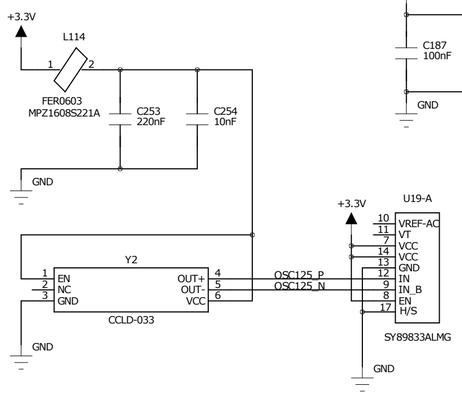
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

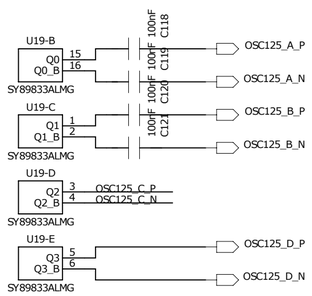


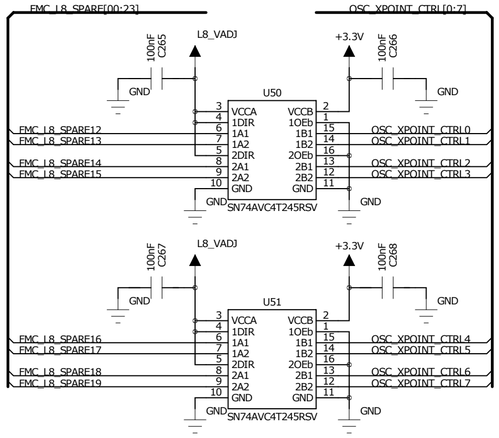


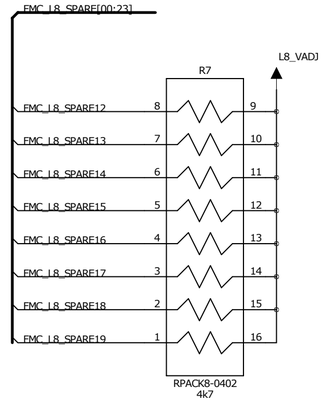








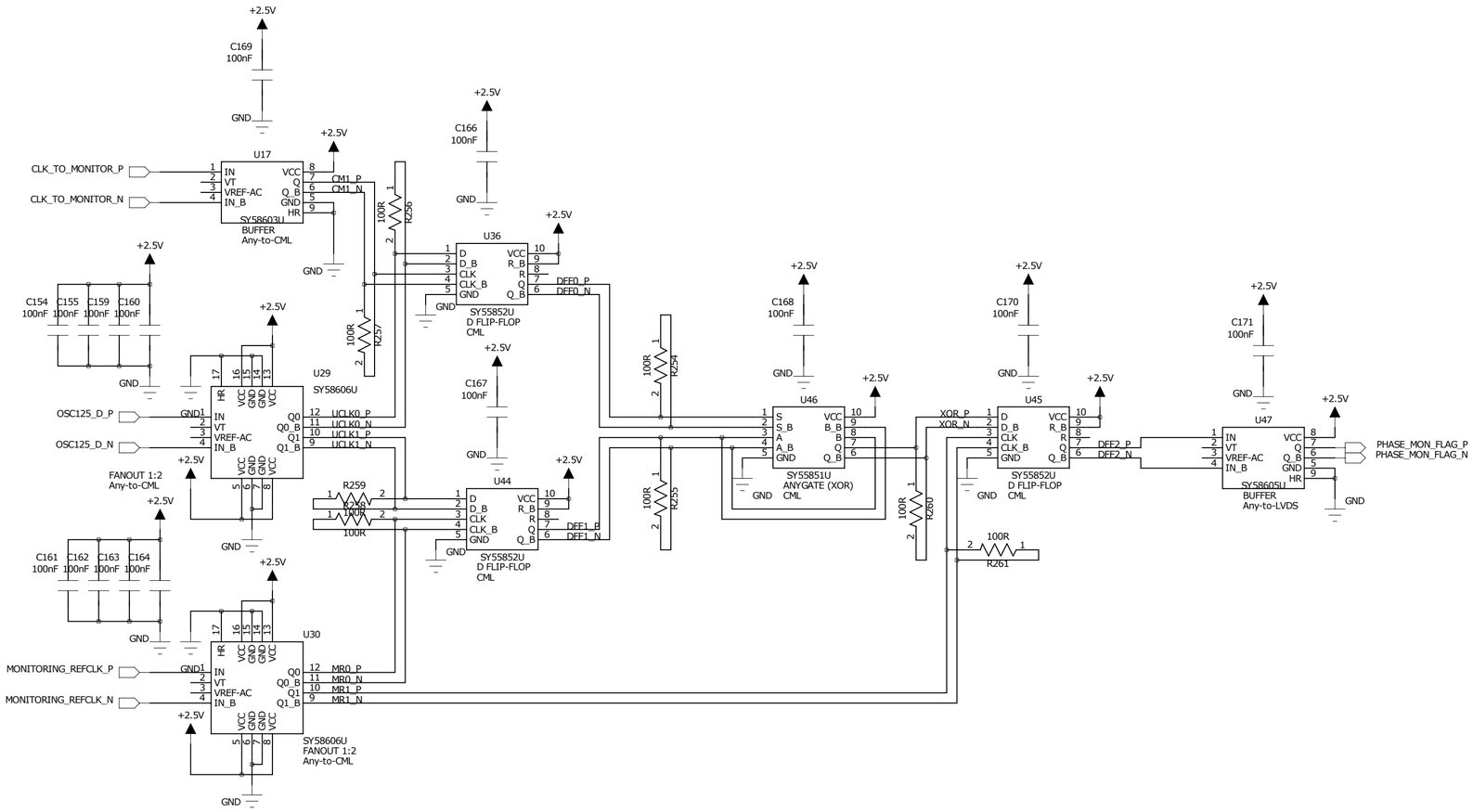




STD PROTOCOL CLOCKING

DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: CLK_DIST_STD	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 9 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



TTC MGT CLOCK PHASE MONITORING

COMPANY: Imperial College/CERN					
TITLE: CLK_DIST_MON					
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	CODE: <Code>	SIZE: A2	DRAWING NO: FC7-R2	REV: v37
CHECKED: <Checked By>	DATED: <Checked Date>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 10 of 26	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Series termination near CPLD

Bank1

C340 220nF, C341 220nF, C342 220nF, C343 220nF, C344 220nF, C345 220nF, C346 220nF, C347 220nF — +3.3V — GND

Bank2

C348 220nF, C349 220nF, C350 220nF, C351 220nF, C352 220nF, C353 220nF, C359 220nF, C360 220nF — +3.3V — GND

C384 2.2uF — +3.3V — GND

AMC_JTAG_CONTROL

*** Place 33 ohm resistors close to CPLD ***

MP7_R1 Mod, Greg
TriState to +3.3V

D26 TRICOLOR_LED_RA: ANODE, RED R39 150R, GREEN R44 120R, BLUE R334 48R7 — +3.3V

R328 100k — SW1 SWITCH_KSC441J70SH-LFS — GND

R150 100k — C165 10uF 10V 0603 — GND

Y4 ASEMPC: VDD, GND, TRI_STATE, OUT — C869 100nF — +3.3V — GND

UC_FPGACLK

FMC_L12_PRSNT_L

FMC_L8_PRSNT_L

Note: 100MHz oscillator can consume 30mA so runs on payload power

UC_GPIO0, UC_GPIO1, UC_GPIO2, UC_GPIO3 — UC_GPIO[0:7]

SPI_DQ0, SPI_DQ1, SPI_DQ2, SPI_DQ3, SPI_SCLK, SPI_CS_B — R29 33R

UC_EBI_D[0:15]: UC_EBI_D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0

UC_EBI_A[0:19]: UC_EBI_A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0

UC_EBI_NWE_1, UC_EBI_NWE_0, UC_EBI_NRD, UC_EBI_NCS_1

UC_EBI_D15, D14, D13, D12, D11

U25-A: XC2C256-6FTG256C

VCCIO1 J6, K6, L7, L8, J11, K11, L10, L9

FB5_MC1 R1, FB5_MC2 N4, FB5_MC3 N2, FB5_MC4_GCK1 M3, FB5_MC5 P1, FB5_MC6_GCK0 M2, FB5_MC12 L3, FB5_MC13 N1, FB5_MC14 L4, FB5_MC15 M1, FB5_MC16 L5, FB6_MC1 N3, FB6_MC2_CDRST P2, FB6_MC3 P4, FB6_MC4_GCK2 P5, FB6_MC5 R2, FB6_MC6 T1, FB6_MC12_DGE T2, FB6_MC13 N5, FB6_MC14 R4, FB6_MC15 M5, FB6_MC16 R5, FB7_MC1 K4, FB7_MC2 L2, FB7_MC3 K3, FB7_MC4 L1, FB7_MC5 K5, FB7_MC6 K2, FB7_MC11 J4, FB7_MC12 K1, FB7_MC13 J3, FB7_MC14 J2, FB7_MC15 J5, FB7_MC16 J1, FB8_MC1 R6, FB8_MC2 N6, FB8_MC3 R3, FB8_MC4 M6, FB8_MC5 T3, FB8_MC6 P6, FB8_MC11 T4, FB8_MC12 P7, FB8_MC13 T5, FB8_MC14 N7, FB8_MC15 R7, FB8_MC16 M7, FB13_MC1 R15, FB13_MC2 T16, FB13_MC3 N14, FB13_MC4 R16, FB13_MC5 N15, FB13_MC6 M15, FB13_MC12 M13, FB13_MC13 P16, FB13_MC14 N16, FB13_MC15 L14, FB13_MC16 M14, FB14_MC1 P15, FB14_MC2 P14, FB14_MC3 P13, FB14_MC4 R13, FB14_MC5 N13, FB14_MC6 R14, FB14_MC12 T15, FB14_MC13 R12, FB14_MC14 N11, FB14_MC15 M11, FB14_MC16 N10, FB15_MC1 L15, FB15_MC2 L13, FB15_MC3 M12, FB15_MC4 M16, FB15_MC5 K14, FB15_MC6 L16, FB15_MC11 K15, FB15_MC12 L12, FB15_MC13 K16, FB15_MC14 J14, FB15_MC15 J15, FB15_MC16 J13, FB16_MC1 P10, FB16_MC2 R10, FB16_MC3 T10, FB16_MC4 R9, FB16_MC5 N9, FB16_MC6 M8, FB16_MC11 T8, FB16_MC12 P8, FB16_MC13 R8, FB16_MC14 T7, FB16_MC15 N8, FB16_MC16 T6

UC_JTAG_TDI R147 33R
UC_JTAG_TMS R148 33R
UC_JTAG_TCK R149 33R
UC_JTAG_TDO

AMC_JTAG_TCK, AMC_JTAG_TDI, AMC_JTAG_TMS, AMC_JTAG_TDO — R133 33R

HEADER_JTAG_CONTROL

JTAG Connector
Top view
Notch next to pin 7

J4-1	pin2 = power	J4-2	
J4-3	pin4 = tms	J4-4	
J4-5	pin6 = tck	J4-6	
J4-7	pin8 = tdo	J4-8	
J4-9	pin10 = tdi	J4-10	
J4-11	pin12 = nc	J4-12	NC
J4-13	pin14 = nc	J4-14	NC

R144 10k, R143 10k, R130 10k, R83 10k, R131 10k — +3.3V — GND

R146 33R

R145 10k — GND

R38 RPACK8-0402 33R

FMC_L12_TDI, FMC_L12_TCK, FMC_L8_TDI, FMC_L8_TMS, FMC_L12_TMS

JTAG Connector

Top view
Notch next to pin 7

J3-1	pin2 = power	J3-2	
J3-3	pin4 = tms	J3-4	
J3-5	pin6 = tck	J3-6	
J3-7	pin8 = tdo	J3-8	
J3-9	pin10 = tdi	J3-10	
J3-11	pin12 = nc	J3-12	
J3-13	pin14 = nc	J3-14	

R141 10k, R138 10k — +3.3V — GND

*** Place 33 ohm resistors close to CPLD ***

R151 33R — +1.8V, +3.3V

R142 10k — GND

U25-C: XC2C256-6FTG256C

TCK P12, TDI R11, TDO A10, TMS N12, VCCAUX_JTAG P4, VCC P3, VCC K13, VCC D12, VCC D5, GND F11, GND F6, GND G10, GND G7, GND G8, GND G9, GND H10, GND H7, GND H8, GND H9, GND J10, GND J7, GND J8, GND J9, GND K10, GND K7, GND K8, GND K9, GND L11, GND L6, GND

NC A1, NC C2, NC E6, NC D1, NC E1, NC G2, NC F1, NC G1, NC M2, NC T9, NC P9, NC M9, NC M10, NC T11, NC T12, NC T13, NC P11, NC T14, NC J16, NC K12, NC D16, NC G12, NC C15, NC D14, NC D6, NC C6, NC E7, NC C5

Bank2

U25-B: XC2C256-6FTG256C

VCCIO2 F7, F8, G6, H6, F10, F9, H11

FB1_MC1 B3, FB1_MC2 B4, FB1_MC3_GSR C4, FB1_MC4 A2, FB1_MC5 A3, FB1_MC6 A4, FB1_MC12 B5, FB1_MC13 A5, FB1_MC14 B6, FB1_MC15 C7, FB1_MC16 D3

FPGA_MODE_2, FPGA_MODE_0, FPGA_MODE_1

FB2_MC1_GTS2 C3, FB2_MC2 E3, FB2_MC3_GTS3 B2, FB2_MC4 D4, FB2_MC5_GTS0 D2, FB2_MC6 E5, FB2_MC12_GTS1 B1, FB2_MC13 E4, FB2_MC14 C1, FB2_MC15 E2, FB2_MC16 A6

R294 33R — FPGA_CCLK
R293 33R — FPGA_FCS_B
R296 33R — FPGA_RDWR_B
FPGA_CSI_B
FPGA_PROG_B
FPGA_INIT_B
R17 33R — FPGA_DONE
R78 33R — FPGA_EMC_CLK
FPGA_CPLD_CLK

Use open drain for FPGA_PROG_B
Use open drain for FPGA_INIT_B

FB3_MC1 D7, FB3_MC2 B7, FB3_MC3 E9, FB3_MC4 A7, FB3_MC5 D8, FB3_MC6 B8, FB3_MC12 C8, FB3_MC13 A8, FB3_MC14 E11, FB3_MC15 E10, FB3_MC16 F2

FB4_MC1 F3, FB4_MC2 G4, FB4_MC3 G3, FB4_MC4 F5, FB4_MC5 G5, FB4_MC6 H2, FB4_MC12 H4, FB4_MC13 H3, FB4_MC14 H1, FB4_MC15 H5, FB4_MC16 B13

R135 33R — CPLD2FPGA_EBI_NWE_1
R273 33R — CPLD2FPGA_EBI_NWE_0
R274 33R — CPLD2FPGA_EBI_NRD
R288 33R — CPLD2FPGA_EBI_NCS_1

FB9_MC1 B14, FB9_MC2 C13, FB9_MC3 A15, FB9_MC4 C12, FB9_MC5 B12, FB9_MC6 D13, FB9_MC11 A14, FB9_MC12 E13, FB9_MC13 A13, FB9_MC14 C11, FB9_MC15 A12, FB9_MC16 A16

CPLD2FPGA_CONFIG_DATA05, CPLD2FPGA_CONFIG_DATA04, CPLD2FPGA_CONFIG_DATA03, CPLD2FPGA_CONFIG_DATA02, CPLD2FPGA_CONFIG_DATA00, CPLD2FPGA_CONFIG_DATA01, CPLD2FPGA_CONFIG_DATA06, CPLD2FPGA_CONFIG_DATA07

CPLD2FPGA_CONFIG_DATA[00:15]

FB10_MC1 B15, FB10_MC2 C14, FB10_MC3 G11, FB10_MC4 B16, FB10_MC5 D15, FB10_MC6 E14, FB10_MC11 C16, FB10_MC12 F14, FB10_MC13 F13, FB10_MC14 E15, FB10_MC15 G13, FB10_MC16 B11

R117 33R — CPLD2FPGA_GPIO3
R118 33R — CPLD2FPGA_GPIO2
R119 33R — CPLD2FPGA_GPIO1
R120 33R — CPLD2FPGA_GPIO0

CPLD2FPGA_GPIO[0:3]

33R resistors close to CPLD

FB11_MC1 D11, FB11_MC2 A11, FB11_MC3 D10, FB11_MC4 B10, FB11_MC5 E12, FB11_MC6 F12, FB11_MC11 B9, FB11_MC12 C9, FB11_MC13 C10, FB11_MC14 A9, FB11_MC15 D9, FB11_MC16 F15

CPLD2FPGA_CONFIG_DATA08, CPLD2FPGA_CONFIG_DATA09, CPLD2FPGA_CONFIG_DATA10, CPLD2FPGA_CONFIG_DATA11, CPLD2FPGA_CONFIG_DATA12, CPLD2FPGA_CONFIG_DATA13, CPLD2FPGA_CONFIG_DATA14, CPLD2FPGA_CONFIG_DATA15

33R resistors close to CPLD

FB12_MC1 G14, FB12_MC2 E16, FB12_MC3 H12, FB12_MC4 F16, FB12_MC5 H16, FB12_MC6 G15, FB12_MC11 H13, FB12_MC12 G16, FB12_MC13 H14, FB12_MC14 H15, FB12_MC15 J12, FB12_MC16

R120 33R — FPGA_JTAG_TDI
R121 33R — FPGA_JTAG_TMS
R122 33R — FPGA_JTAG_TCK
FPGA_JTAG_TDO

FMC_L12_TDO

R319 33R — FMC_L8_TCK
FMC_L8_TDO

XC2C256-6FTG256C

R161 1K, R178 1K, R180 1K, R184 1K, R335 1K, R336 1K, R337 1K, R338 1k — +3.3V

J1-A, J1-B, J1-C, J1-D, J1-E, J1-F, J1-G, J1-H

GND

VCCAUX

+3.3V — C361 220nF, C362 220nF, C363 220nF, C364 220nF, C365 220nF — GND

VCC

+1.8V — C366 220nF, C367 220nF, C368 220nF, C369 220nF, C370 220nF — GND

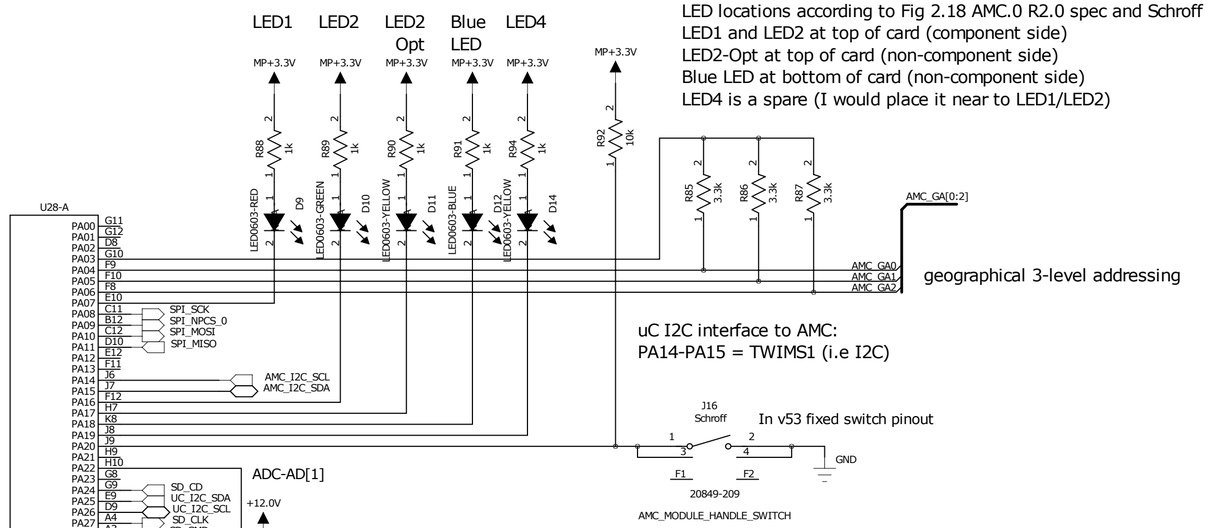
Managment Power (~100mA)

Heat disipation not a problem < 100mW, but check thermal dissipation

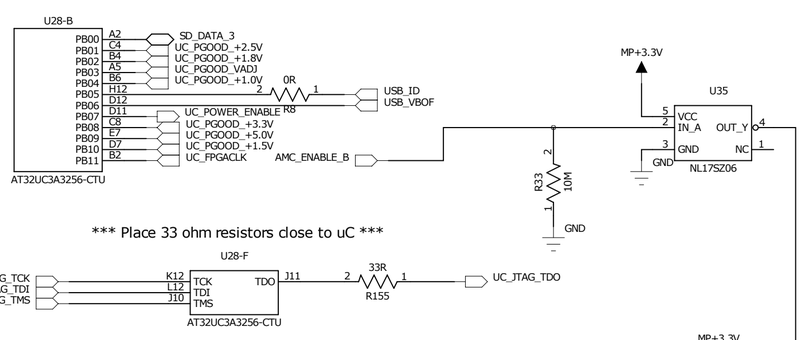
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: CPLD	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
SCALE: <Scale>		SHEET: 11 OF 26	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

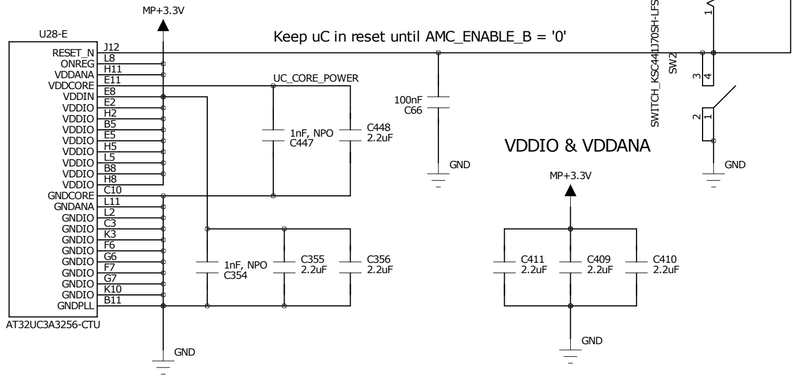
LED locations according to Fig 2.18 AMC.0 R2.0 spec and Schroff "AMC-MODULE_LIGHTPIPE.pdf"
LED1 and LED2 at top of card (component side)
LED2-Opt at top of card (non-component side)
Blue LED at bottom of card (non-component side)
LED4 is a spare (I would place it near to LED1/LED2)

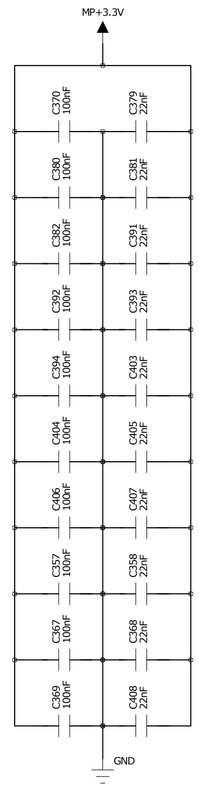


Reserved PA27-PA31 and PB00-PB04 for MCI Interface (e.g FlashCard)
According to spec enable_b line from amc ought to be inverted to create reset_b signal...
USART, I2C, DAC and ADC all available from uC header (not all at same time)
LEDs in right location, but net names wrong. No longer display net names
uC now not directly connected to manual reset switch/pwr on



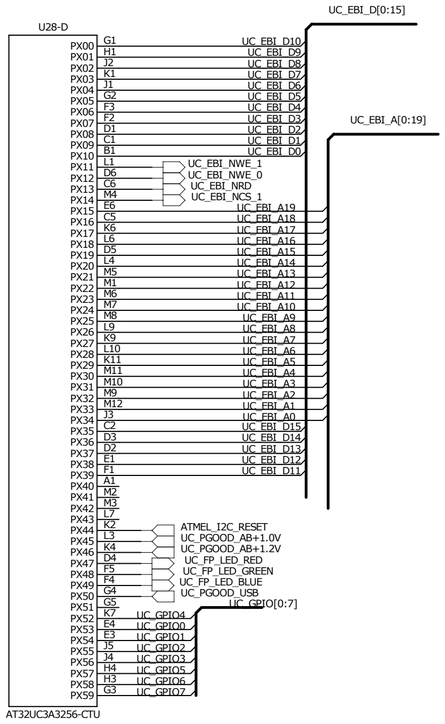
There is one 22nF/0.1uF cap per VDDIO or VDDANA pin
The 1nF between VDDCORE and GNDCORE should be close to the pins.
The 1nF between VDDIN and GNDCORE should be close to the pins.

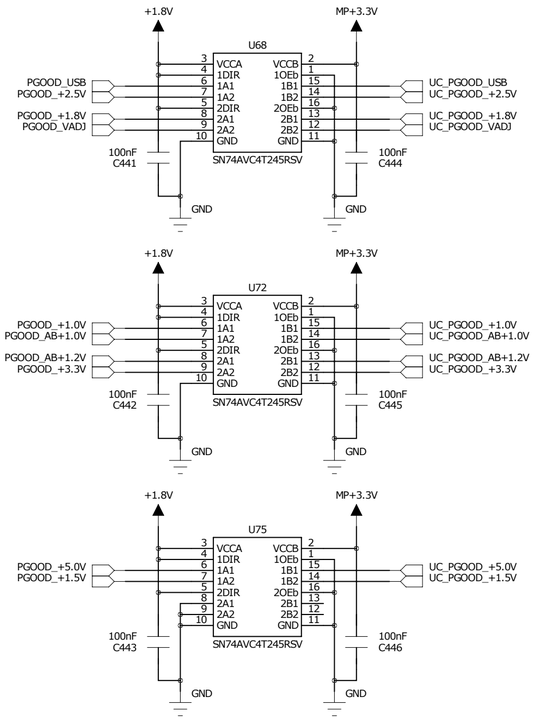


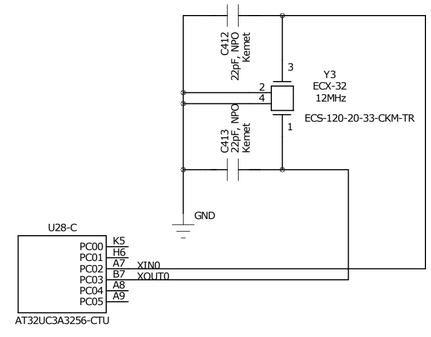


VDDIO & VDDANA

Inverting buffer required
Open drain acceptable
U14 deleted ,U35+R33 added _Sarah 8.5.12







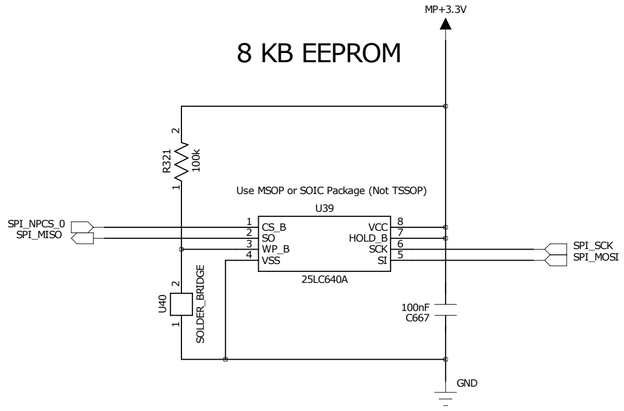
Main Clock

Use EIA Class 1 dielectric or part number specified for crystal caps

COMPANY: Imperial College/CERN			
TITLE: UC			
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: FC7-R2	REV: v37
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 12 OF 26

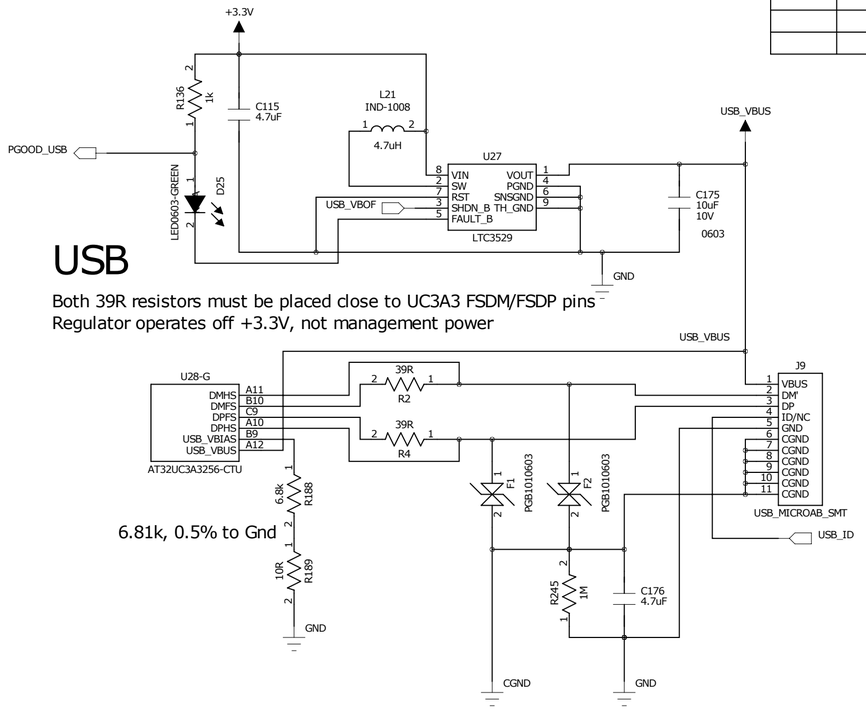
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

8 KB EEPROM

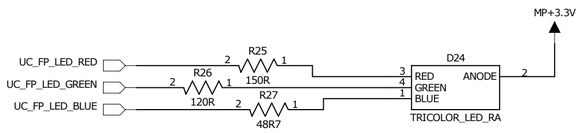


USB

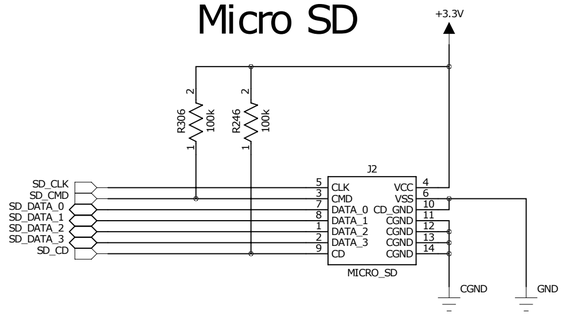
Both 39R resistors must be placed close to UC3A3 FSDM/FSDP pins
Regulator operates off +3.3V, not management power



MP7_R1 Mod, AWR
Green Res->120R

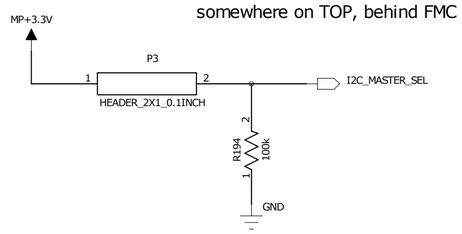


Micro SD



Better to have this on MP?

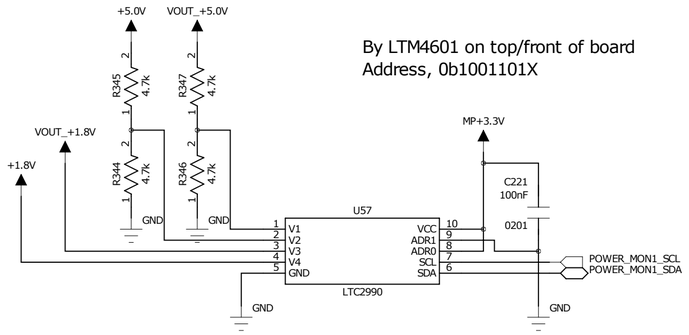
I2C Bus Master Jumper
somewhere on TOP, behind FMC L8



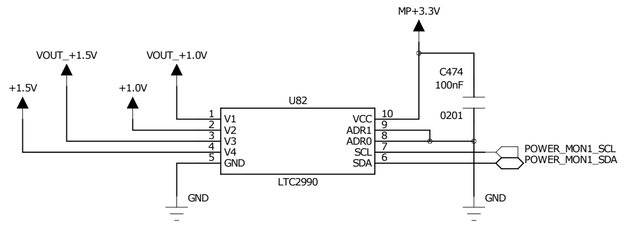
COMPANY: Imperial College/CERN			
TITLE: UC_PERIPHERALS_1			
DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: FC7-R2	REV: v37
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 13 OF 26

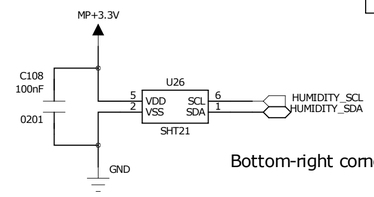
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

By LTM4601 on top/front of board
Address, 0b1001101X



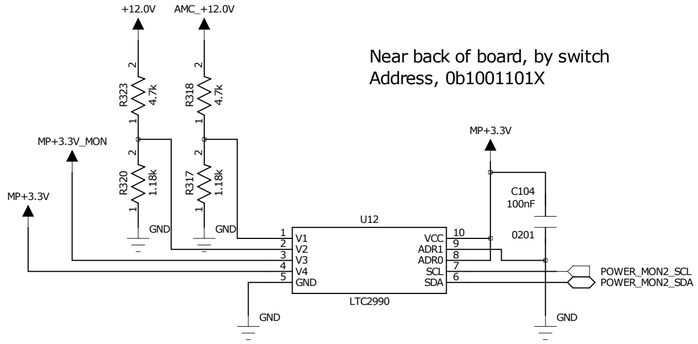
By LTM4601s on top of board
Address, 0b1001100X



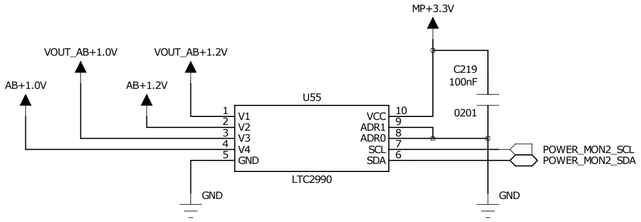


Bottom-right corner of board, use cutout for thermal isolation
Address 0b1000000X

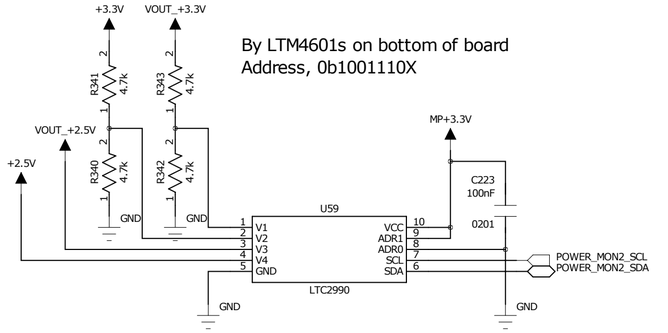
Near back of board, by switch
Address, 0b1001101X



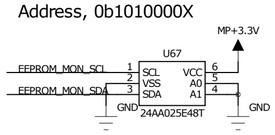
By LTM4606s on back of board
Address, 0b1001100X

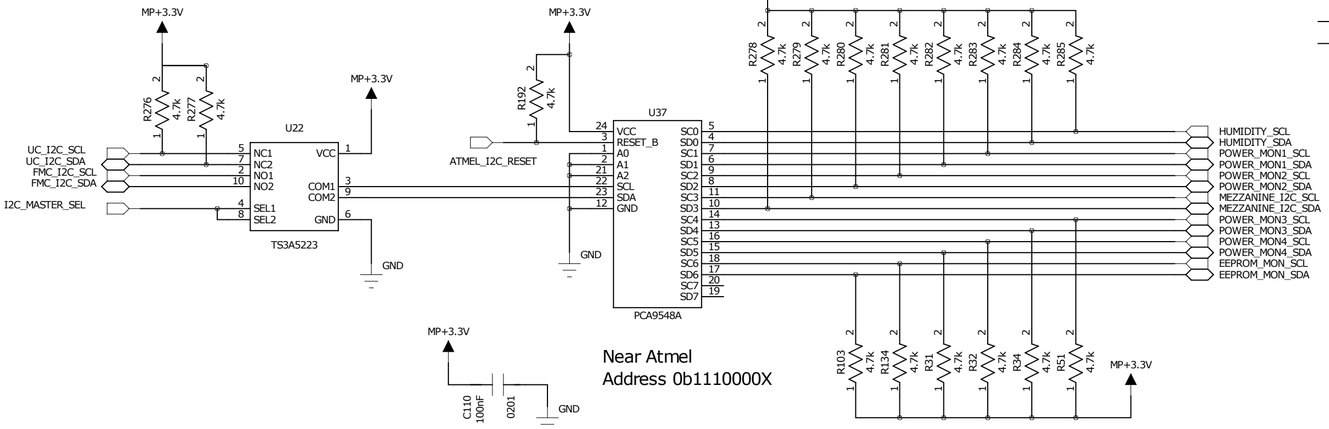


By LTM4601s on bottom of board
Address, 0b1001110X



Address, 0b1010000X





Near Atmel
Address 0b1110000X

Voltage, current and temperature monitors on:

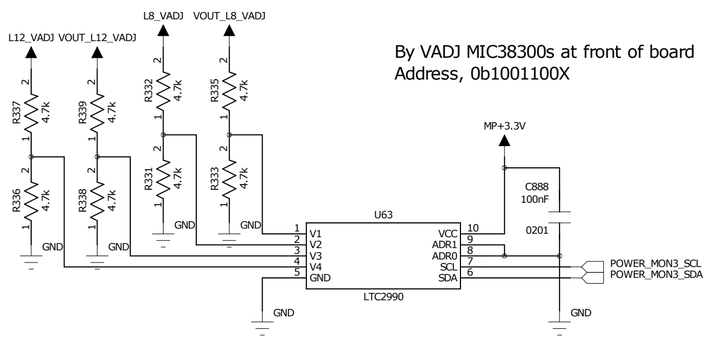
+5.0V, +1.8V
+1.0V, +1.5V
+12V AMC, +3.3V MP
+1.2V GTX, +1.0V GTX
+3.3V, +2.5V
VADJ_L8, VADJ_L12
+1.8V GTX, FPGA TEMP

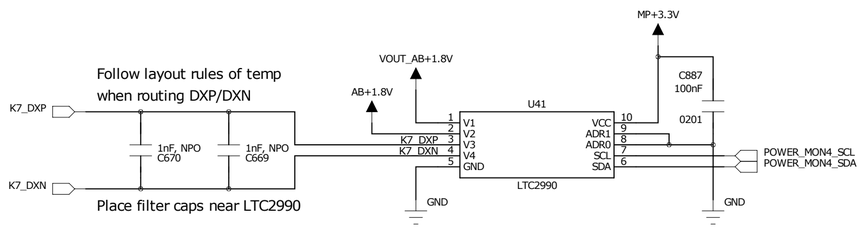
EUID48 EEPROM

Humidity sensor
LTC2990: 1.1 mA Type, 1.8mA Max, Low Power Opt

Monitors will need calibration by MMC when current = 0

By VADJ MIC38300s at front of board
Address, 0b1001100X





Near back MIC5319 for GTXs
Address, 0b1001100X

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RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
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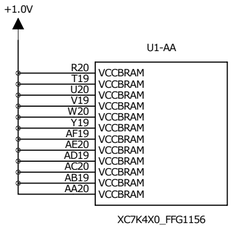
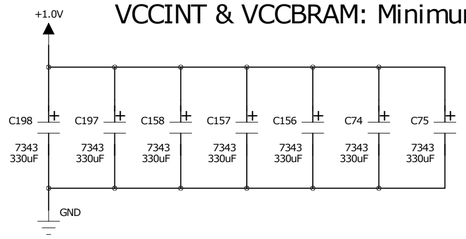
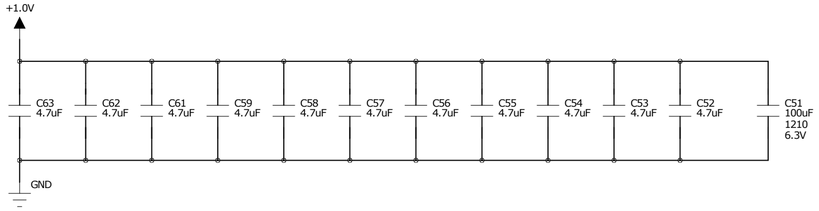
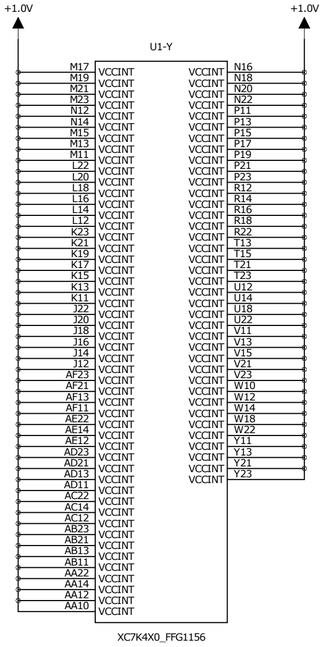
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



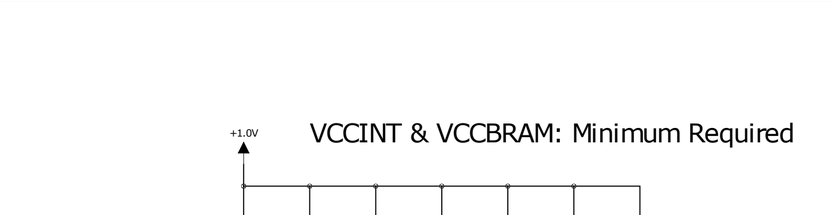


VCCINT & VCCBRAM: Minimum Required

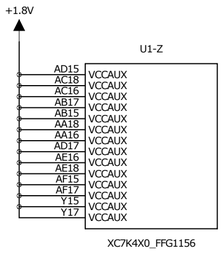


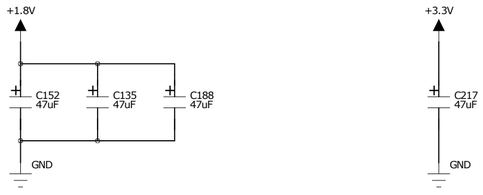


decoupling for XC7K480T part



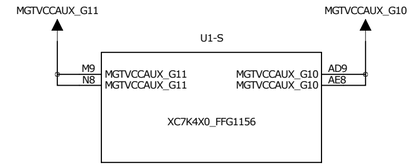
VCCO_X: Minimum Required

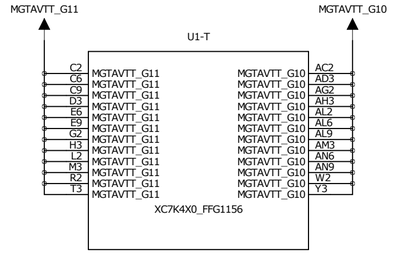


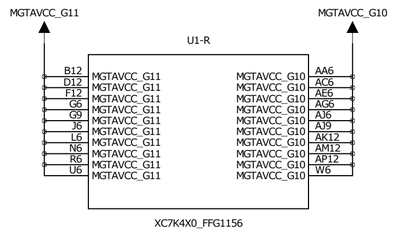


VCCAUX: Minimum Required

VCCO_0: Minimum Required







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RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
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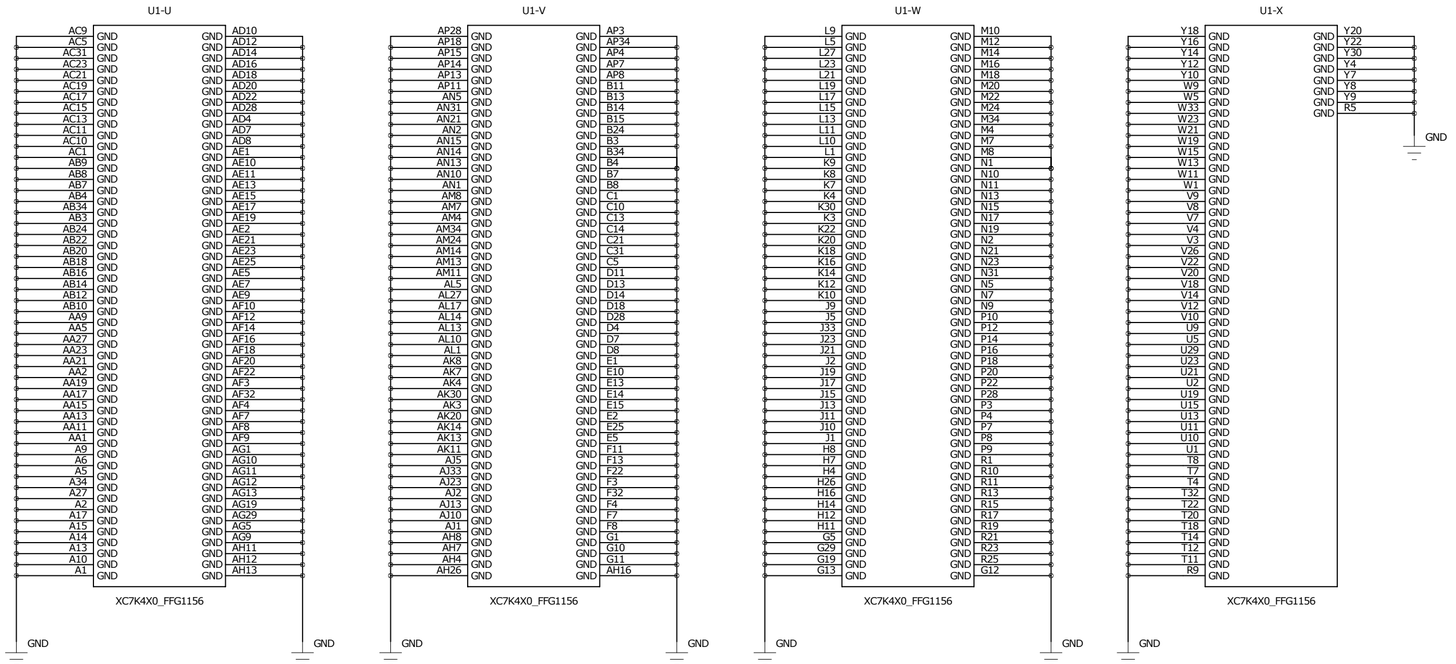
LTR	ECO NO:	APPROVED:	DATE:



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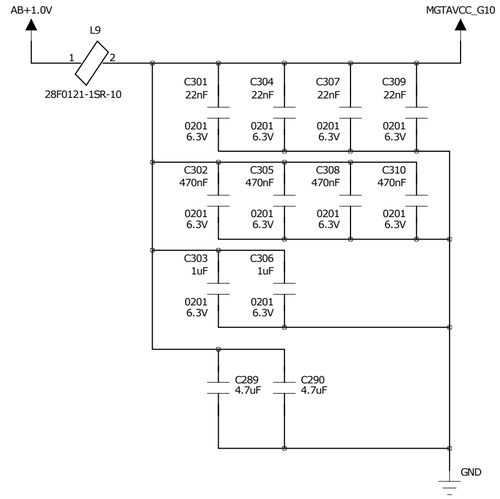

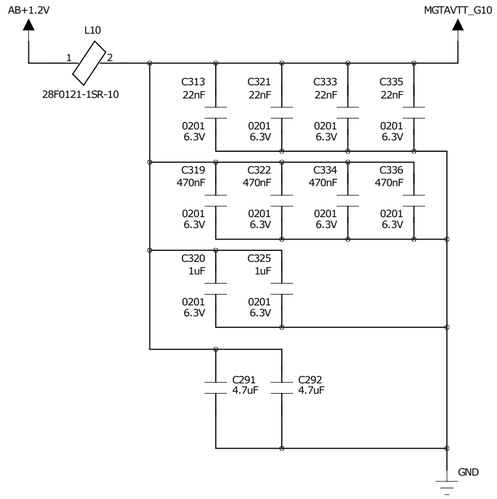

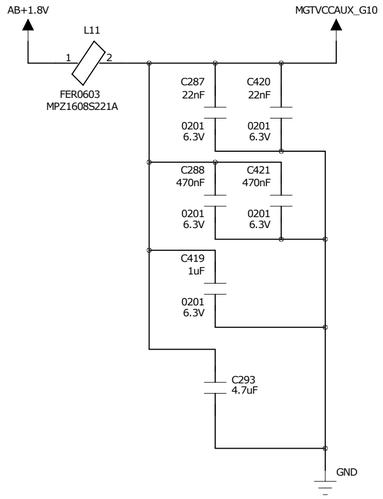

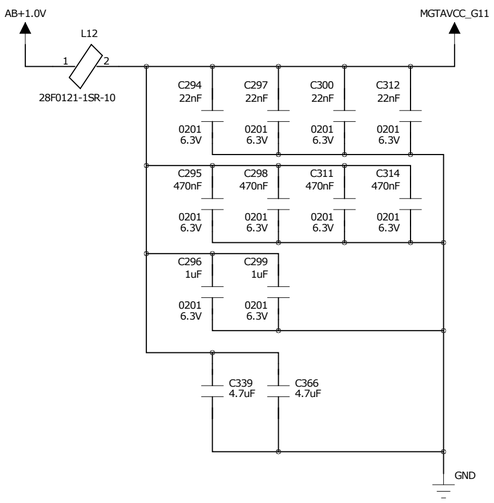

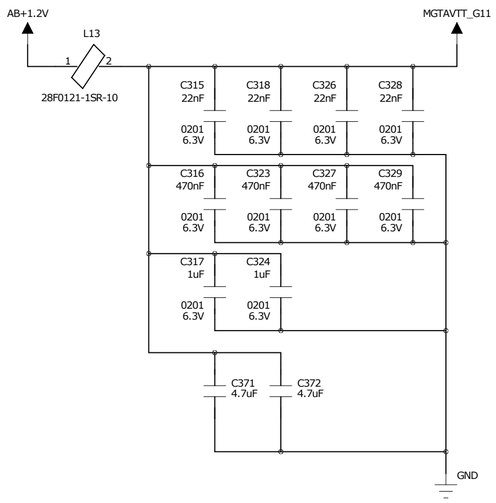

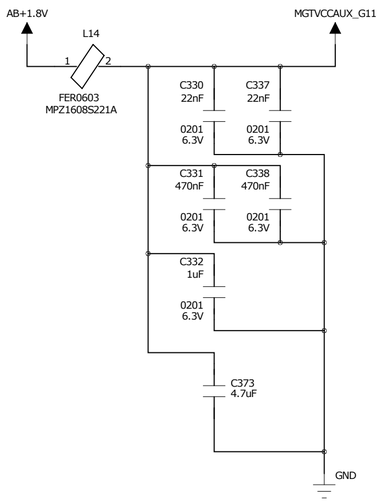

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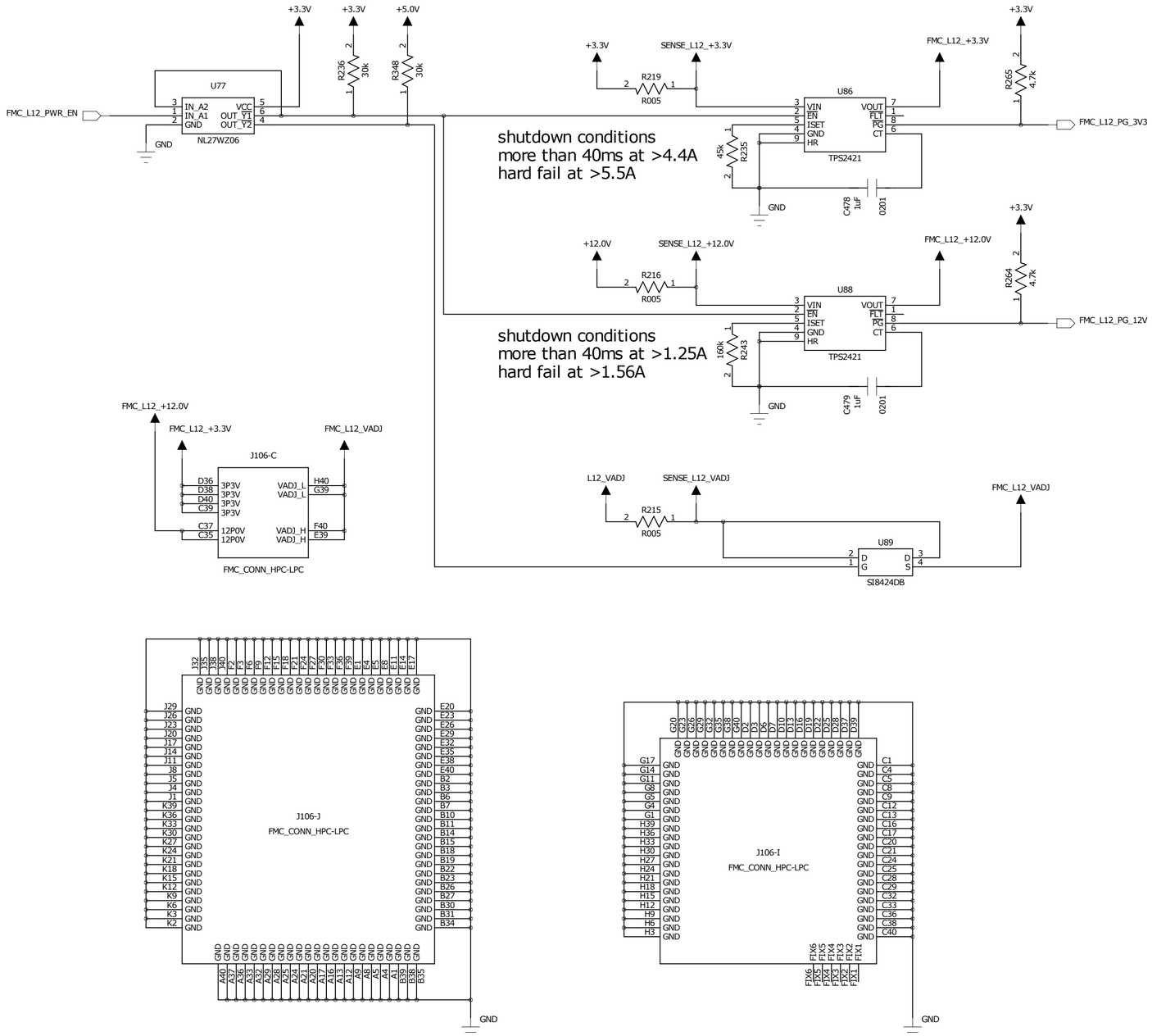
		SCALE: <Scale>	SHEET: 17 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FMC +12V, +3.3V, VADJ supply gating logic
place close to L12 FMC connector/sense resistors



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TITLE:	FMC_L12_POWER		
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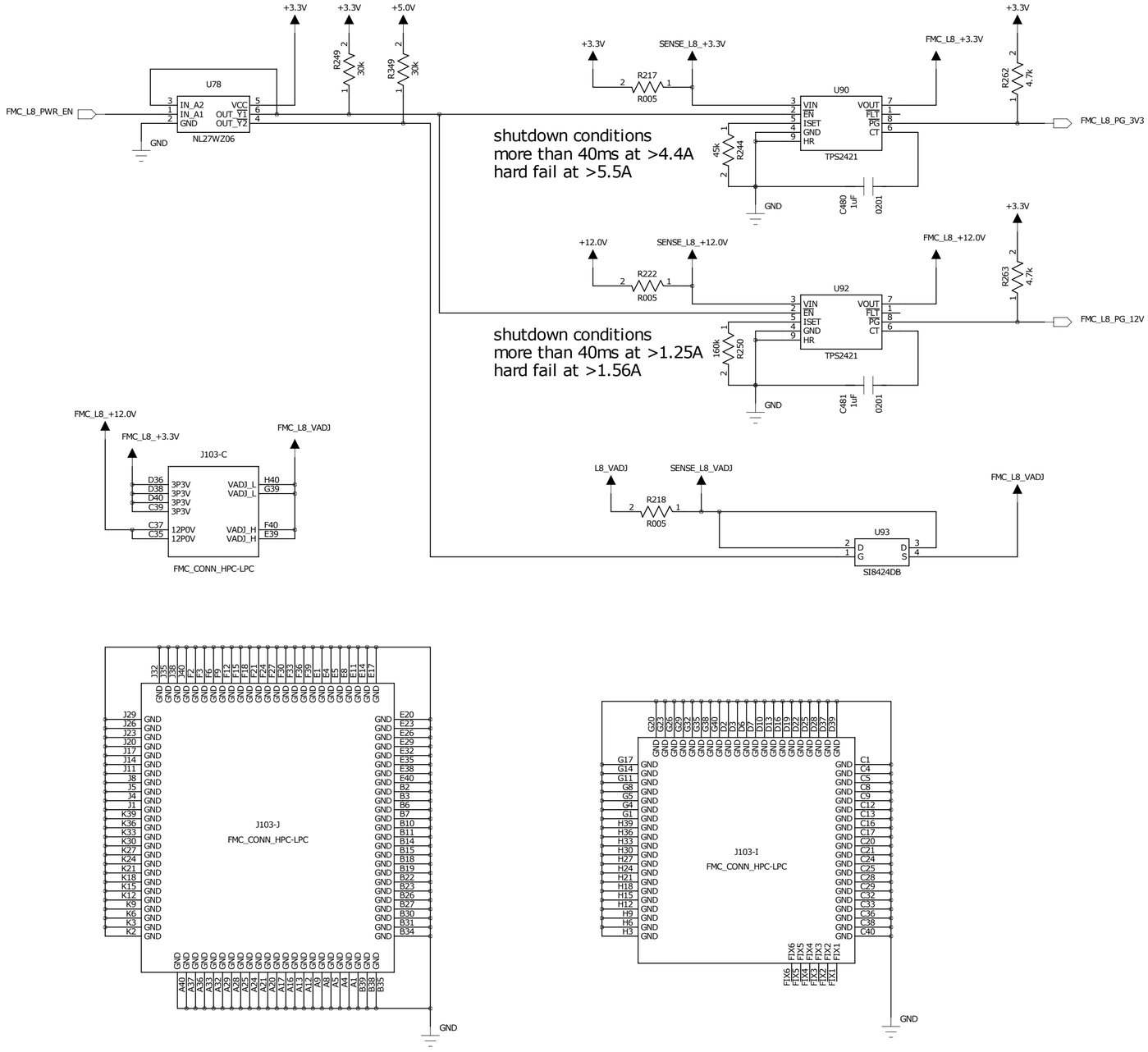
RELEASED: <Released By>	DATED: <Release Date>		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FMC +12V, +3.3V, VADJ supply gating logic
place close to L8 FMC connector/sense resistors



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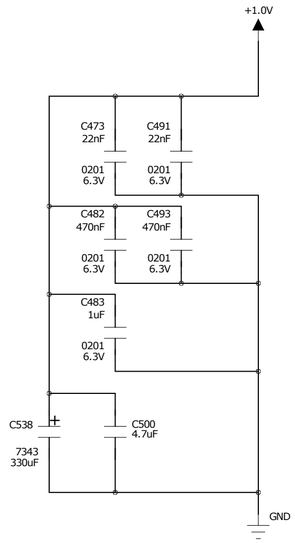
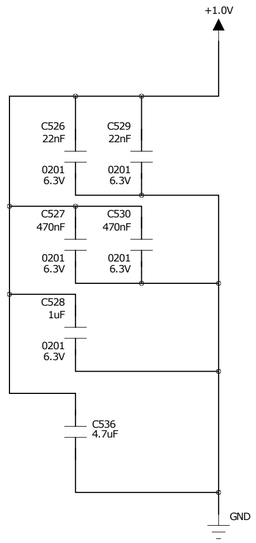
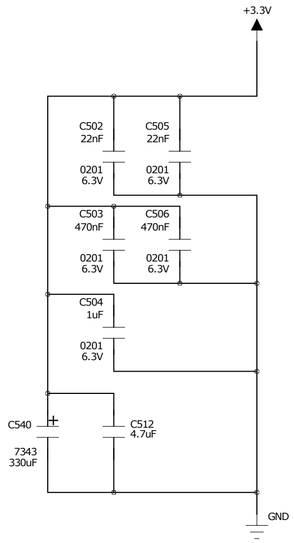
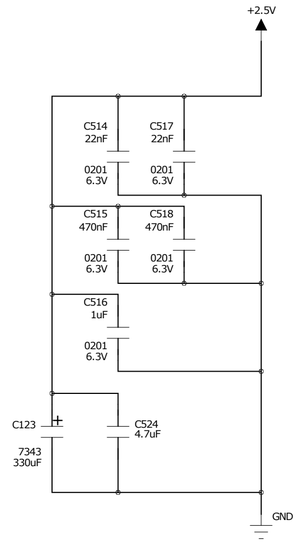
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

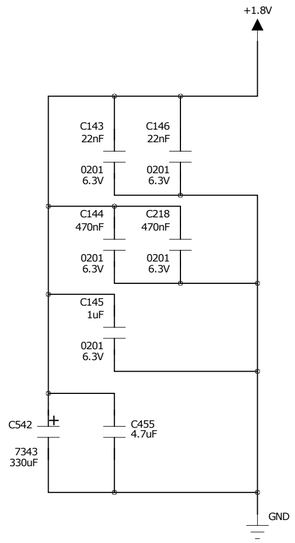
additional main supply decoupling





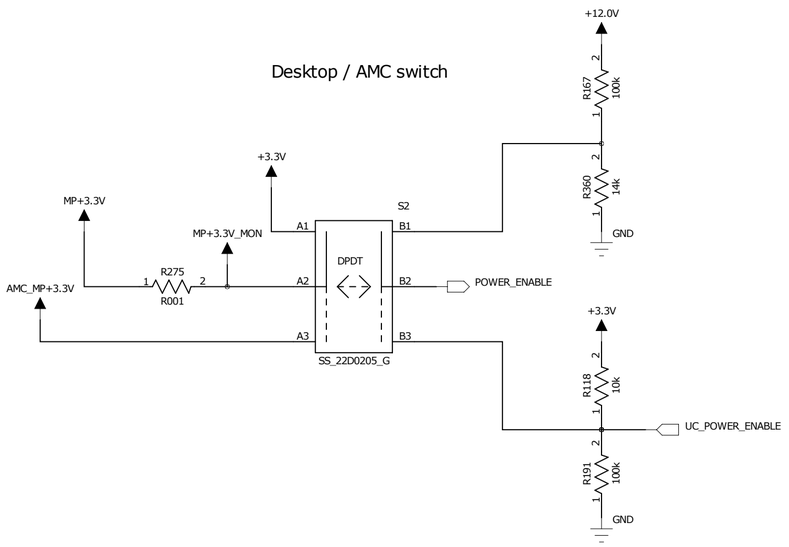


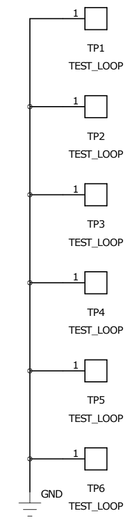


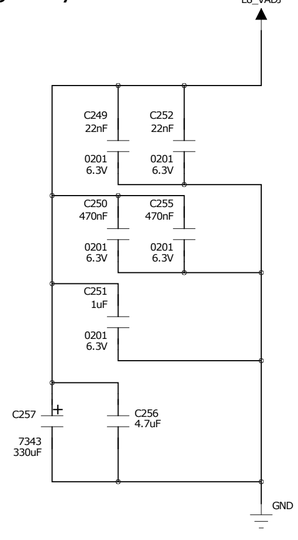


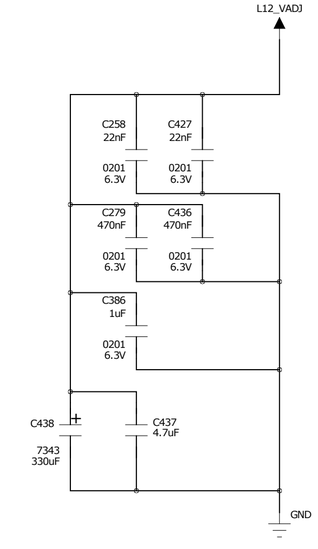
try to fit each network as close to each ferrite/sense resistor as possible

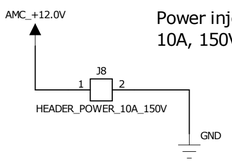
there is one 330uF tant per power supply - can go anywhere

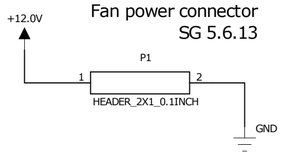












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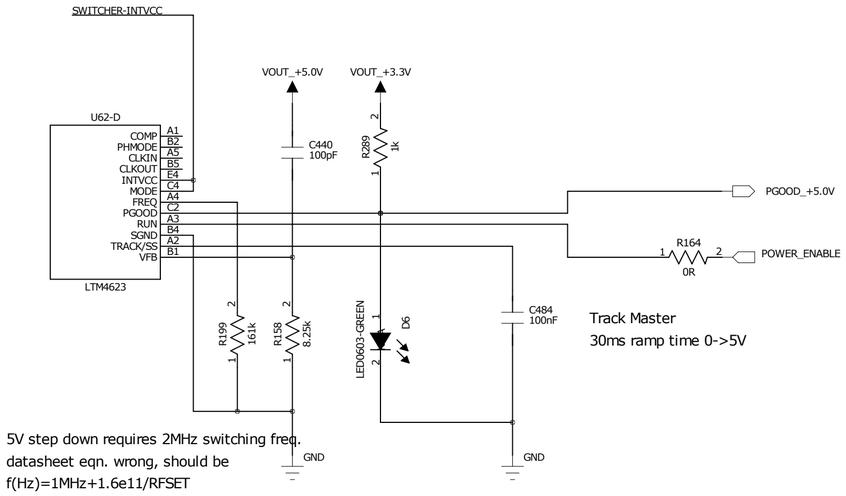
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 20 OF 26

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

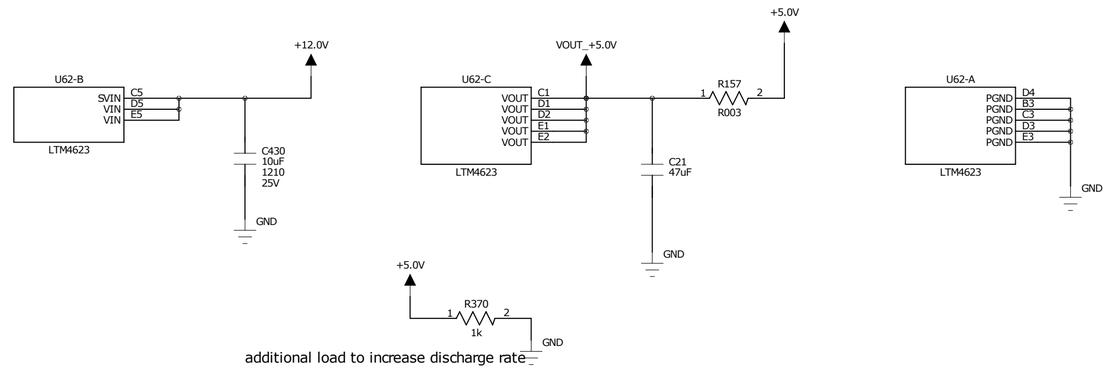
5V, 3A



Track Master
30ms ramp time 0->5V

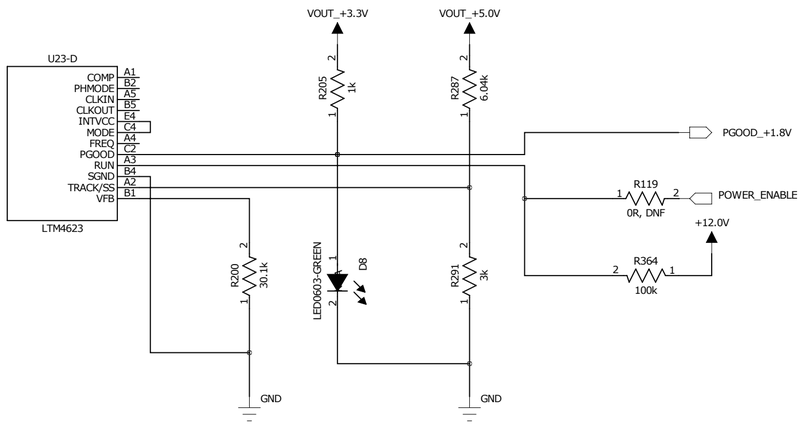
5V step down requires 2MHz switching freq.
datasheet eqn. wrong, should be
f(Hz)=1MHz+1.6e11/RFSET

Use low ESR ceramic caps here

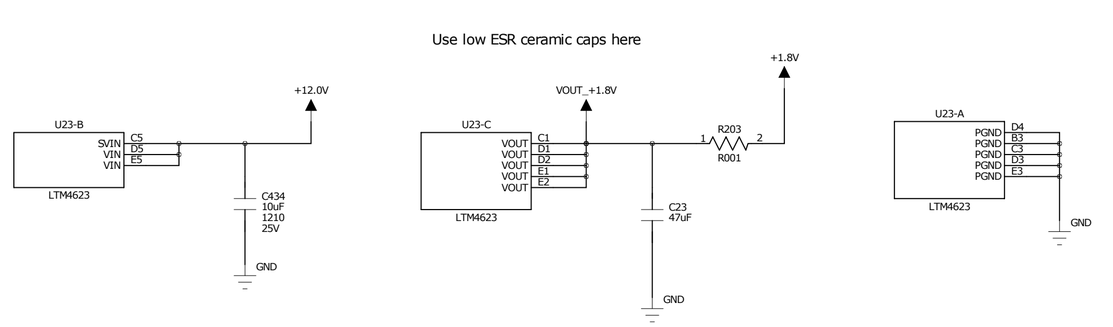


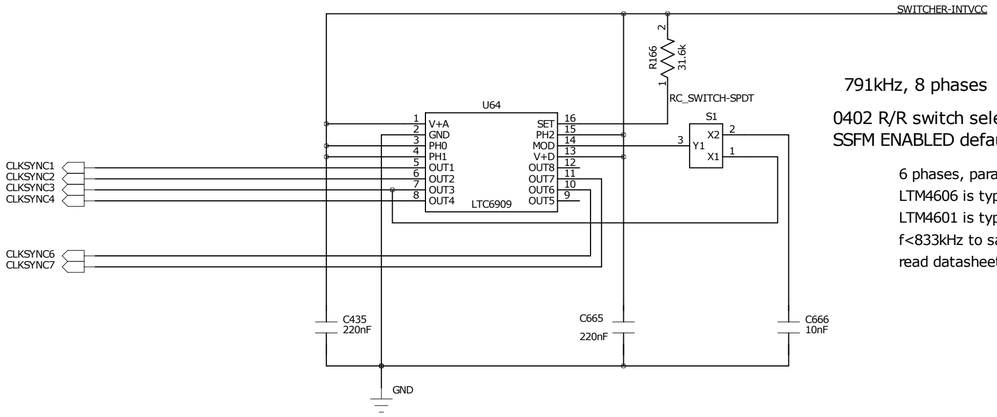
additional load to increase discharge rate

1.8V, 3A



Use low ESR ceramic caps here





791kHz, 8 phases

0402 R/R switch selects SSFM enabled or disabled
SSFM ENABLED default (0R between 1 & 3)

6 phases, parallel 4601s using opposite 180deg phases
LTM4606 is typically 800kHz
LTM4601 is typically 850kHz
f<833kHz to satisfy on time t_on>100ns minimum (for 12V->1V)
read datasheet layout guidelines

DRAWN: P.Vichoudis, M.Pesaresi	DATED: 18.03.2015	COMPANY: Imperial College/CERN	
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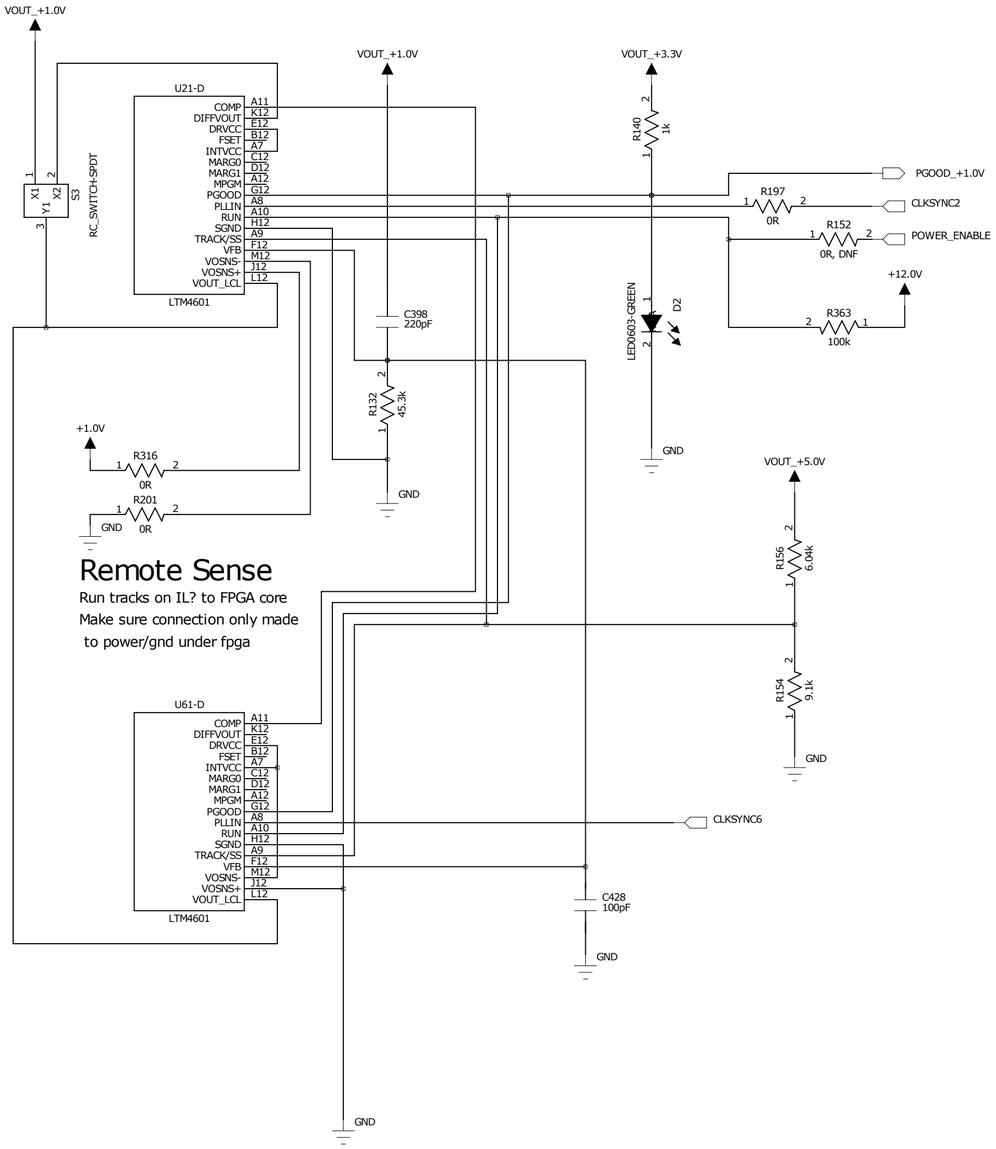
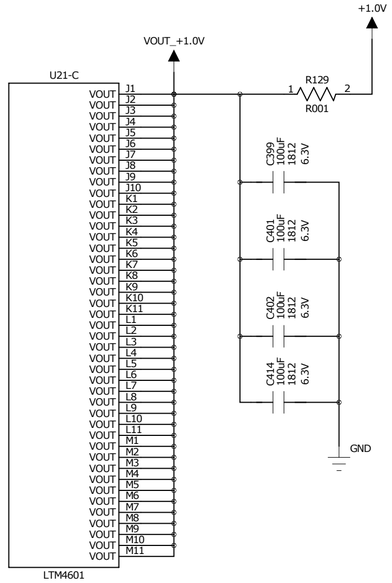
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
		SCALE: <Scale>	SHEET: 21 OF 26

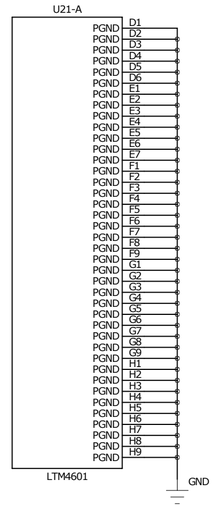
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

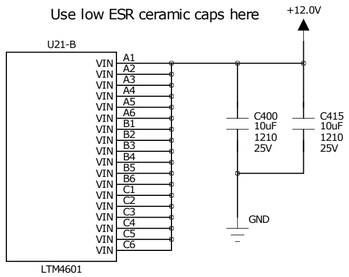
0402 R/R switch selects LOCAL or REMOTE +1.0V feedback
LOCAL sense default (0R between 1 & 3)

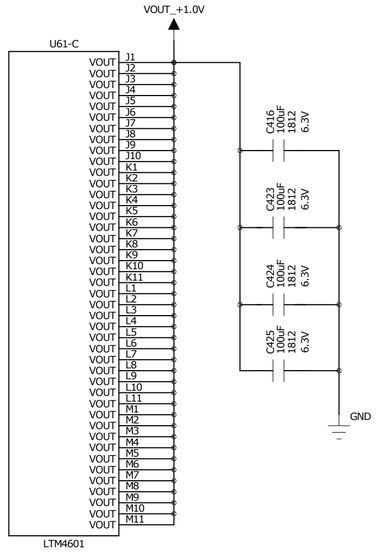
+1.0V, 24A

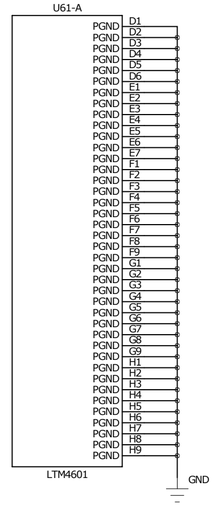


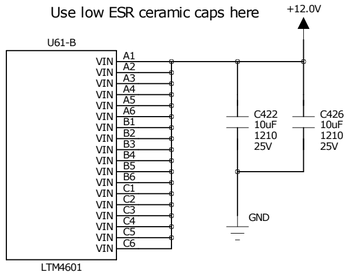












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RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: FC7-R2	REV: v37
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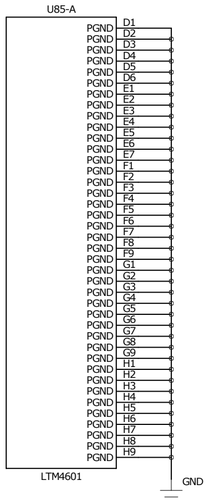
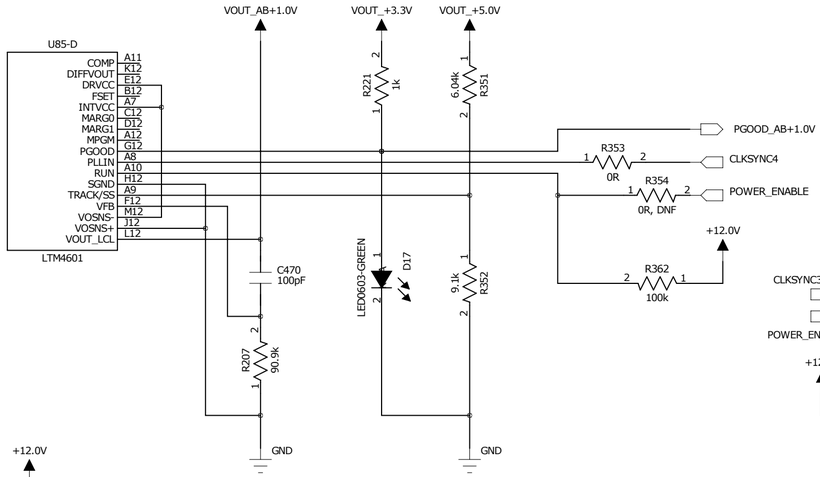
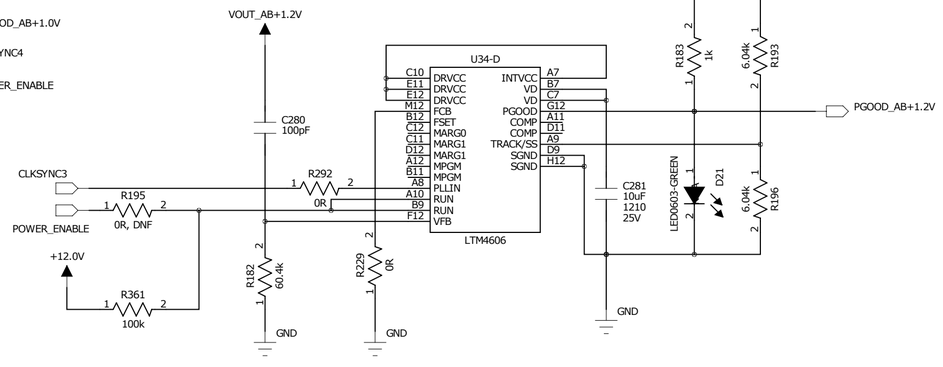
LTR	ECO NO:	APPROVED:	DATE:

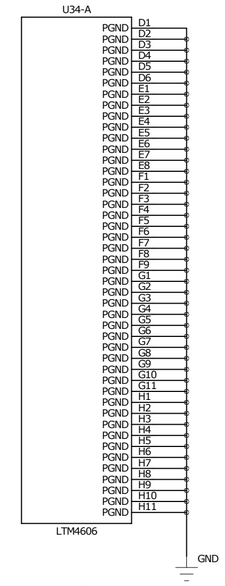
AB+1.0V, 12A



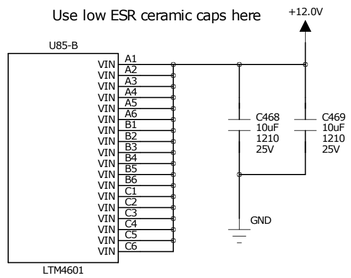


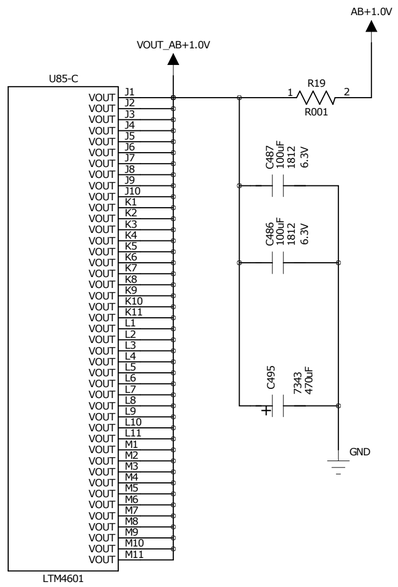
AB+1.2V, 6A



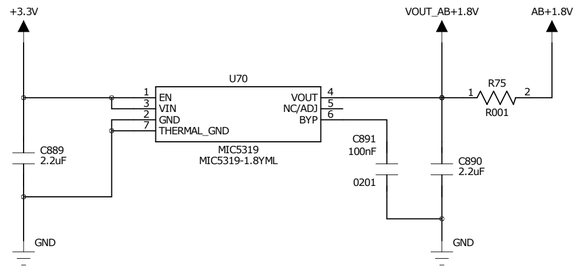


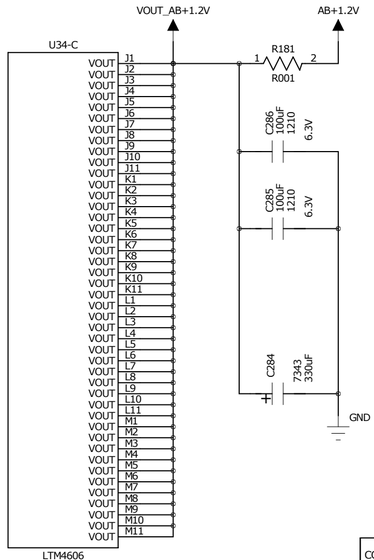
Use low ESR ceramic caps here

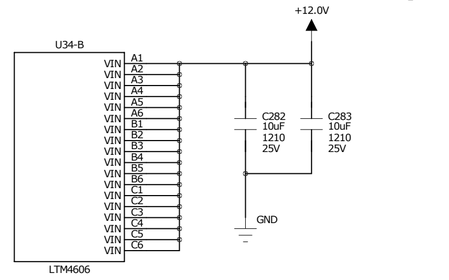


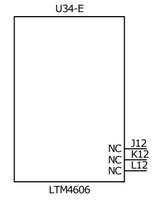


AB+1.8V









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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 23 OF 26

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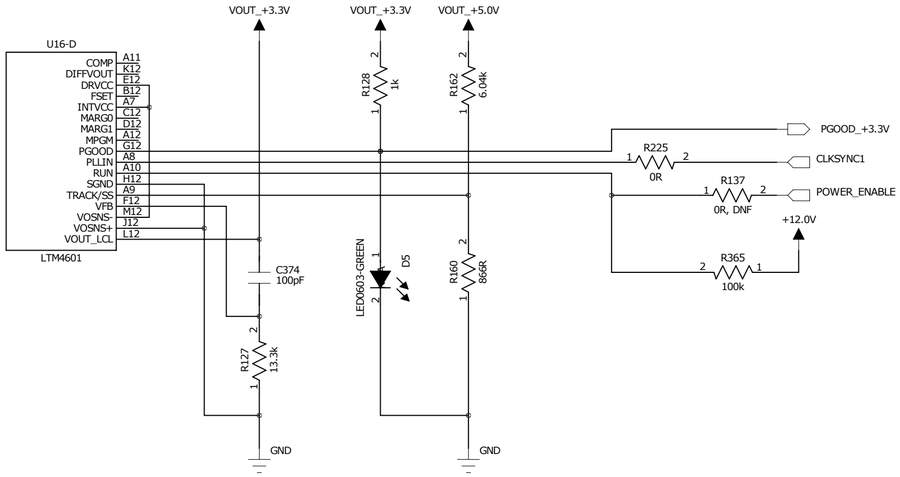
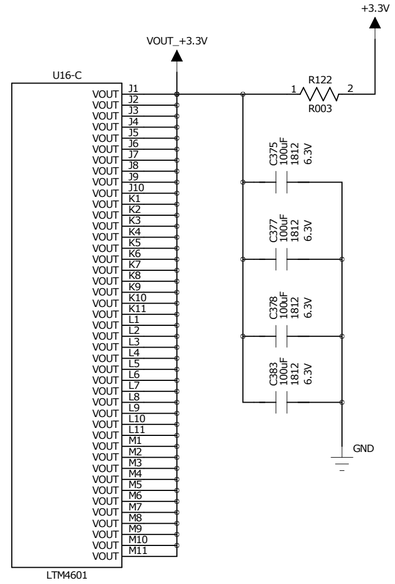
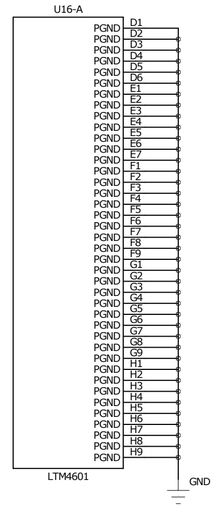
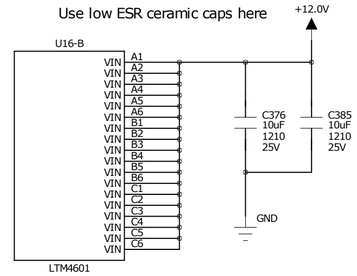
LTR	ECO NO:	APPROVED:	DATE:

+3.3V, 12A

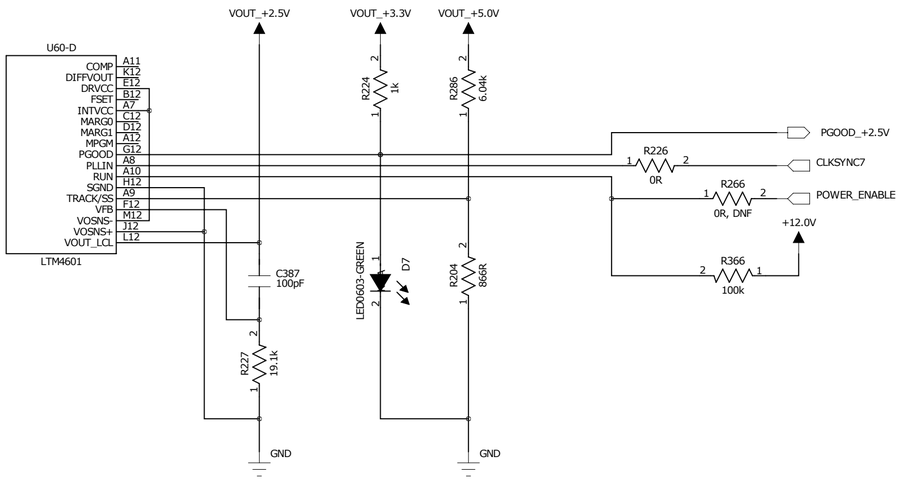


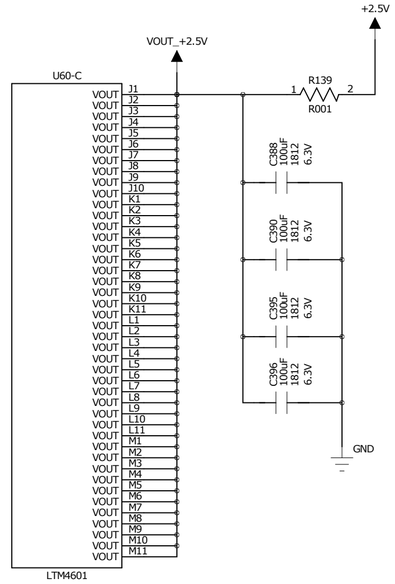


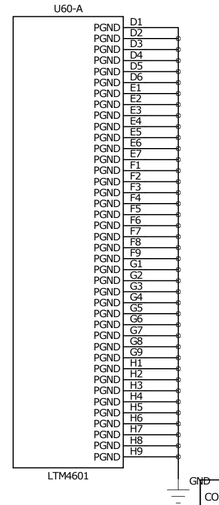


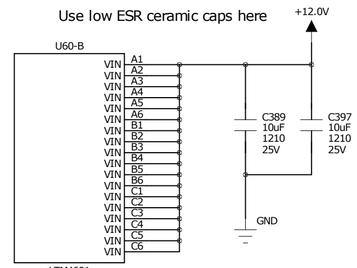


+2.5V, 12A









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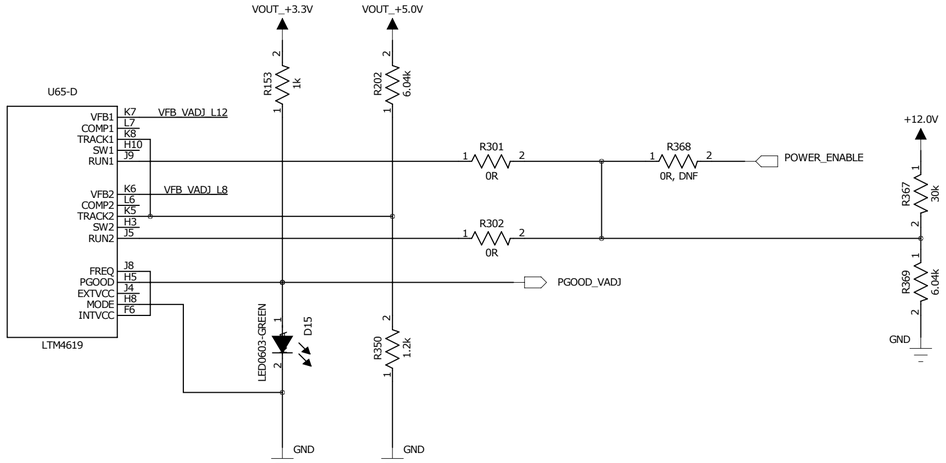
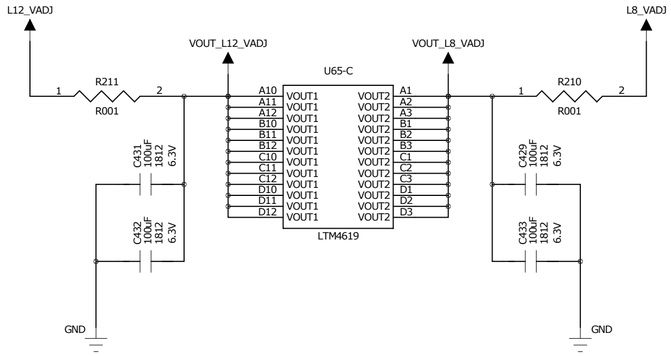
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 24 OF 26	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

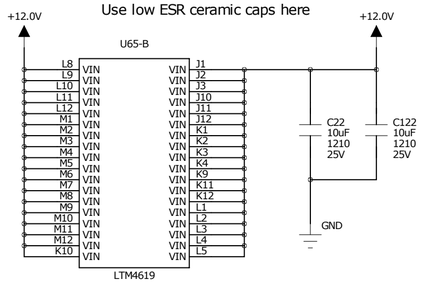
L8_VADJ, 4A
L12_VADJ, 4A

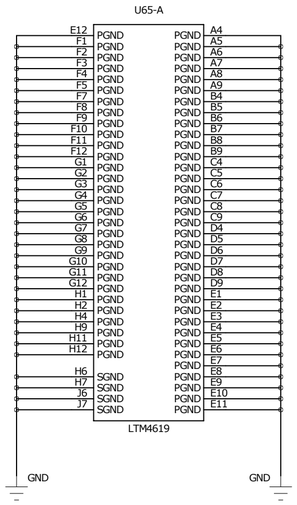


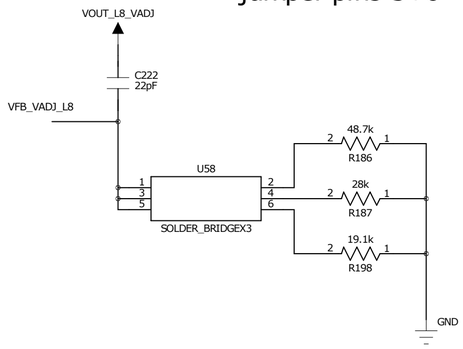


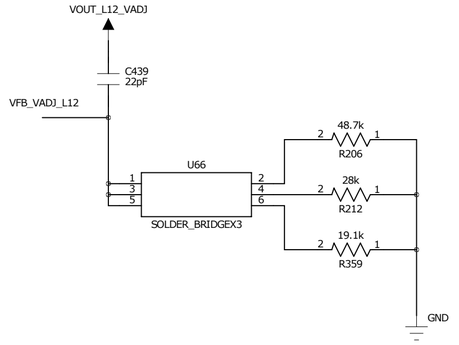
VADJ L8/L12 voltage select

jumper pins 1+2 = 1.8V
jumper pins 3+4 = 2.5V
jumper pins 5+6 = 3.3V









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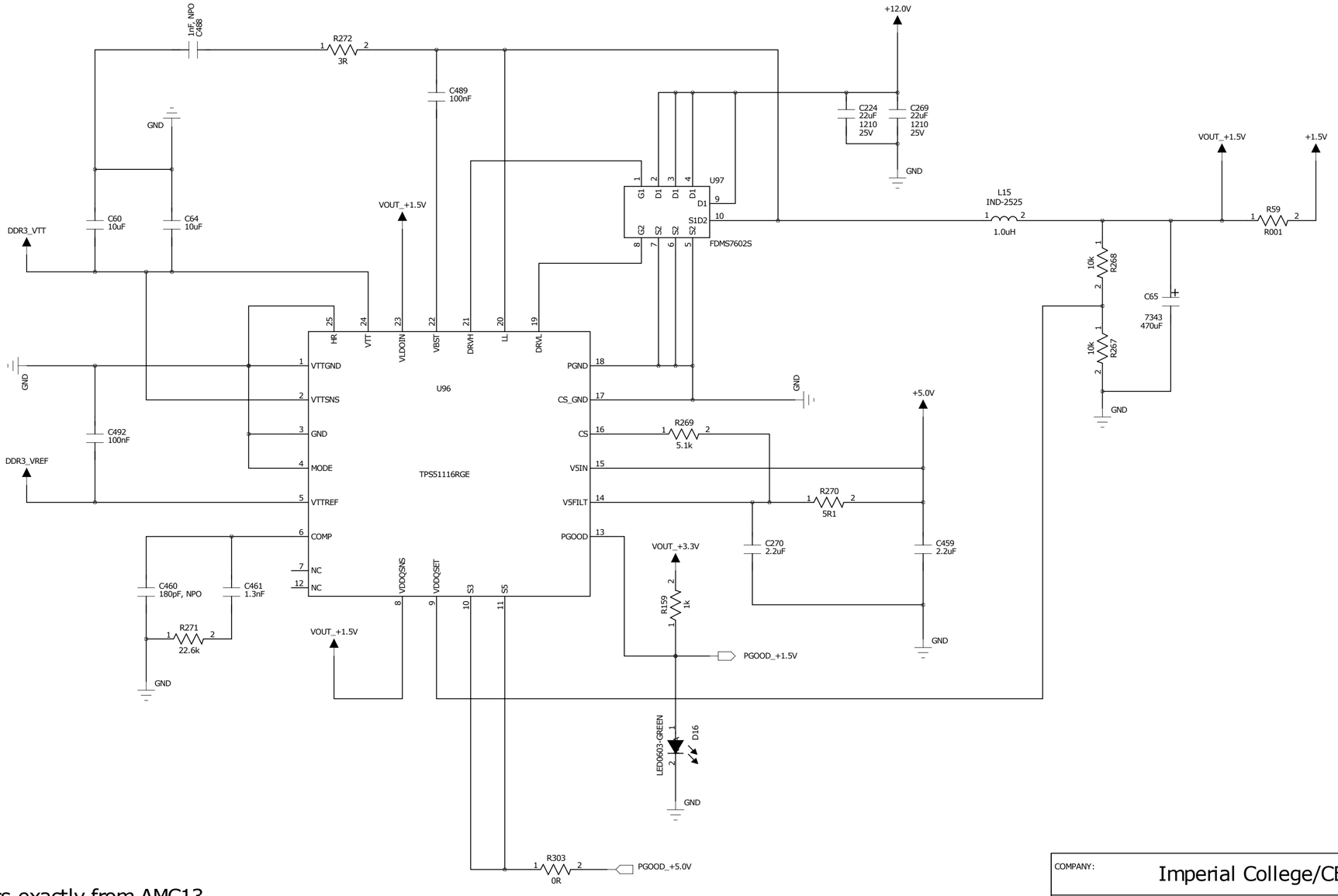
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



schematics exactly from AMC13

follow layout rules from datasheet

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